

SOLDER PASTE SELECTION CHALLENGES FOR BOTTOM TERMINATION COMPONENTS (BTC) ATTACH

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ABSTRACT

Bottom Terminated Component (BTC) use has become extensive in electronic assembly, especially the use of Quad Flat No-lead (QFN) packages. Low cost and small size with improved thermal and electrical performance make BTC components very attractive for many applications.

Implementation of BTC components come with challenges. The low standoff, large central thermal pad and lack of leads result in co-planarity issues due to board warpage and Coefficient of Thermal Expansion (CTE) mismatch. Low standoff and a large central pad may favor increased voiding compared to other package designs. The differences in shape, size, and orientation between the large central/thermal pad and small perimeter pads create different demands on the solder paste, making paste deposit volume and shape consistency across the package difficult to achieve. The fine feature apertures are susceptible to skips and insufficient volume. The large open apertures are susceptible to scooping and drag out. This varying demand on the solder paste rheology complicates paste selection requirements.

In this study, two solder paste chemistries and several printing parameters were evaluated in order to achieve consistent solder paste deposition across the assembly. There are tighter tolerance requirement on the solder paste volume due to thinner stencils and the need for consistent solder paste uniformity across the footprint of the part to prevent potential tilting of the lower standoff components. Printing parameters can be adjusted to ensure well defined (no scooping/drag out), defect free deposits on the thermal pad. New solder paste chemistries with improved rheological properties have been formulated to print with lower squeegee blade angle and pressure which mitigates the scooping phenomena typically observed with larger aperture. Lowering squeegee blade angle with these formulations also appears to improve printing quality for all aperture sizes without the increased flux leaching normally associated with lower print angle. Reduction in print pressure and contact angle will reduce wipe frequency and wear on the stencil. Improved formulations result in lower voiding levels and more uniform print deposition across large and small apertures.

Key words: bottom termination components; solder paste; voiding; printing.

INTRODUCTION

In the last several years, the use of BTC packages has skyrocketed. Cost, size and performance improvements are the main drivers. Their significant growth was projected by the iNEMI roadmap. These components offer a small footprint in combination with a very small stand off and low weight. It also offers an interesting I/O distribution along the perimeter of the package and has very good thermal and electrical performance. Such properties and performance characteristics make BTC's one of the most popular semiconductor packages currently on the market.

Leadless BTC packages do not have solder ball spheres but rather metallized terminations or pads and a large heat-dissipation pad under the package. This configuration with an extra internal heat-sink pad adds new requirements for design and assembly. Many devices have unique pad and stencil design requirements for the thermal pad.

Low standoff components with leads such as Quad Flat Pack (QFP), Decawatt Package (DPAK) or Small Outline Integrated Circuit (SOIC) as well as QFN components without leads, have difficulty compensating for distortion from package, co-planarity of the package or board warpage. Therefore, BTC packages require more controls in the design and assembly processes. These requirements add challenges in second level assembly and reliability. Voids or insufficient solder volume within solder joints under the QFN thermal pad can have an adverse effect not only on thermal performance, but more importantly on high speed and RF performances. Insufficient solder volume or voids can increase the current path of the circuit. Solder volume control and void reduction in both leaded (QFP, DPAK) and non-leaded power components (QFN, LCS) is becoming more important as power density continually increases and component packages get smaller.

Typical electronics assemblies today will have a mixture of various types of BTC's as well as other fine feature devices. It is important for new generation solder pastes to perform effectively and deliver consistent paste volume on the wide variety of aperture shapes and sizes utilized today.

This study was initiated in response to the market's increasing demand for higher power density components that require better consistency and reduced defects in BTC types of assembly. Low voiding and better solder volume consistency for solder joints to optimize the thermal and electrical performance of the packages is critical to achieve the required performance of the final assemblies. Novel process modifications are continuously being proposed to improve overall assembly performance and reliability of BTC components such as the use of preforms, stencil design, pad design, via design and reflow optimization. The most common factors affecting printing are stencil technology, aperture design, pad finish, paste type, printing equipment and printing parameters.

One of the key parameters affecting solder joint reliability for BTC components and especially QFNs are solder standoff and fillet. In some cases, component quality, tolerances and manufacturing inconsistency present potential defect opportunities. **Figure 1** shows optical image of a component with traces of over-mold material on the thermal pad. To ensure acceptable solder joint formation with correct bond line thickness (BLT), solder paste deposit volume has to be sufficient without any defects (misprints, scooping, insufficient, etc.).

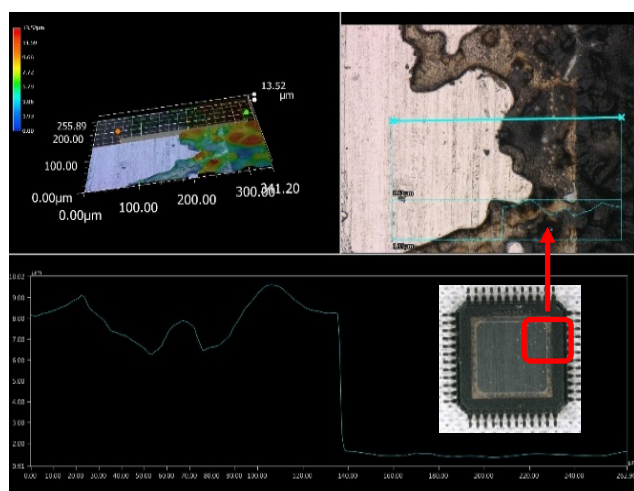


Figure 1. Image of the component with mold compound covering thermal pad (height difference about 10-15 μm).

In some cases, the difference between thermal pad and signal lead height could be up to 50 μm (**Figure 2**), which is still within the component tolerances requirements. With a component presenting this type of height difference between thermal pad and signal leads, solder paste printing quality and consistency across the device footprint with a 4 or 5 mils (100 or 125 μm) stencil becomes critical in order to not adversely affect the final solder joint quality and the overall reliability of the device.

The solder paste printing process is a very complex process that includes several interdependent factors. This study seeks to understand the factors that can contribute to consistent solder volume on the thermal pad as well as

consistent solder deposits on the smaller signal pads with minimal co-planarity variation across the whole device. Printing parameters were varied and their effect on the consistency and quality of the solder deposits was observed and quantified.

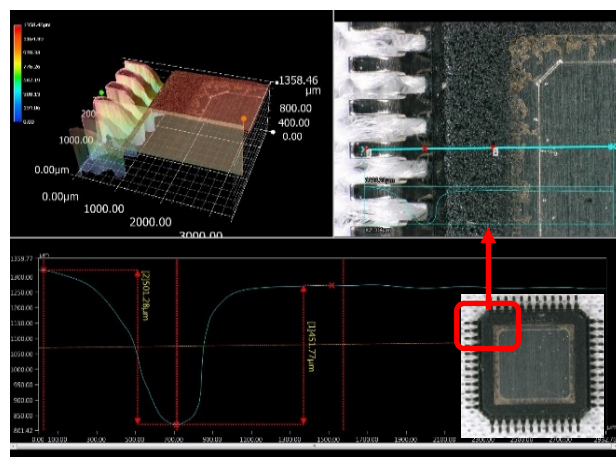


Figure 2. Image of the component with leads and thermal pad at different levels (difference 50-70 μm).

These efforts are focused at developing a solution that maximizes solder volume delivered to the pads, minimizes co-planarity variation across the whole device, while minimizing voiding to generate a high reliability solder joint under bottom termination components.

EXPERIMENTAL PROCEDURE

A full factorial Design of Experiments (DOE) was developed based on key factors contributing to solder volume and voiding under bottom termination components. The effect of printing parameters and solder paste chemistry on the print volume and height consistency were evaluated.

A custom single layer 1.6 mm thick Printed Circuit Board (PCB) test vehicle was designed with a variety of smaller apertures as well as larger thermal pads for this investigation. This design encompassed numerous variables that can contribute to inconsistency in solder deposit for BTC thermal pads and smaller signal pins.

QFN, QFP, LCS and DPAK (**Figure 3.**) components of various sizes and pin configurations were used.

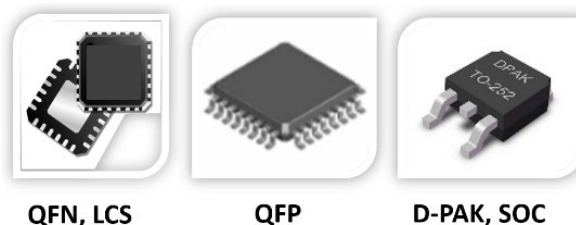


Figure 3. Images of the components.

Two types of solder pastes were selected for evaluation:
 (1) Paste A is an old generation solder paste with good track record for Surface Mount Technology (SMT) performance.
 (2) Paste B is a new generation low voiding solder paste developed for BTC type assembly with improved rheological properties.

The effect of print speed, print pressure and blade angle on performance of old and new generation solder pastes was evaluated. **Figure 4** shows schematics of the print process. **Table 1** shows details of print parameters.

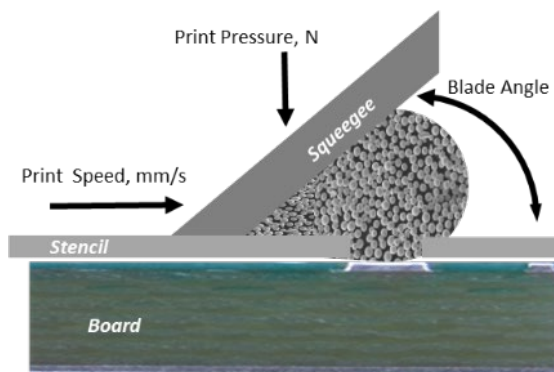


Figure 4. Schematics of the print process and varied parameters.

Table 1. Print process parameters

	Print Speed, mm/s	Print Pressure, N	Blade Angle, Degree
Low	25	54	45
High	100	93	60

An initial evaluation was done on two printers from two different manufactures (Printer 1 and Printer 2). Laser cut stainless steel stencil with rounded corner squared apertures and 4 mil (100 μ m) thickness was used. Based on the results, further evaluation was conducted on Printer 2, which showed more consistent printing performance. This enabled better differentiation between solder pastes and printing parameters.

RESULTS AND DISCUSSION

Print parameters such as print speed, pressure and separation speed can be optimized through process development steps. Print alignment, however, is a function of printer, PCB and stencil. Decoupling the variables is difficult, initial evaluation of the print deposits using the same board design and stencil on two different printers clearly showed solder paste deposition dependence on the printer. This is more applicable for fine feature printing, however, the paste formulation improvements for BTC performance should go along with fine feature printing performance improvements.

The height and area analysis for both printers are shown in **Figure 5**. From inspection, the board support, board-clamping mechanism, and board/stencil gasketing were major factors in solder paste deposit consistency. As the

trend in components and their spacing are rapidly decreases in size, solder paste printing accuracy and solder paste deposit repeatability is becoming critical to a high quality assembly process.

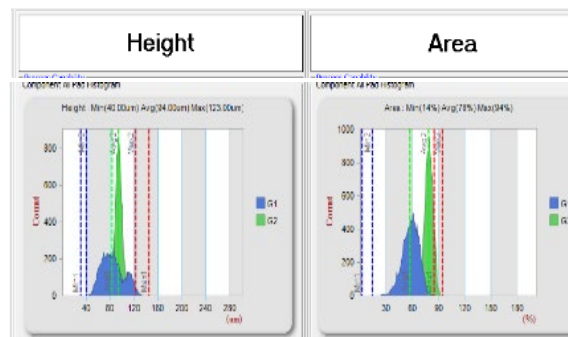


Figure 5. Print height and area measurements using **Printer 1** and **Printer 2**.

Optical and 3D images of the solder pastes for the fine printing deposits (Paste A) on the same location, shown in **Figure 6&7**, demonstrate the variation in deposit shape based on the printer used. Inadequate gasketing of the board and stencil allows the stencil to move during the print stroke resulting in offsetting of the pad and stencil prior to the stencil release from the circuit board. To study the true effect of the printing parameters and different solder paste chemistries on the deposit consistency, including not only the larger thermal pads but also the finer I/O signal leads, all testing was done on Printer 2.

Due to data processing of SPI measurements of fine feature deposits like conical shapes, the area and volume data typically has a bias. It is recommended to engage with SPI equipment suppliers to understand the bias of their equipment as a function of paste deposit shape and size.

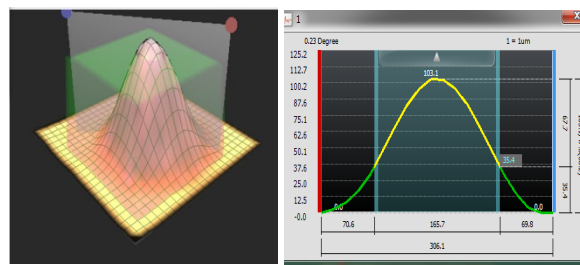


Figure 6. 3D images of Paste A print deposits on the Pad ID4516 printed on **Printer 1**

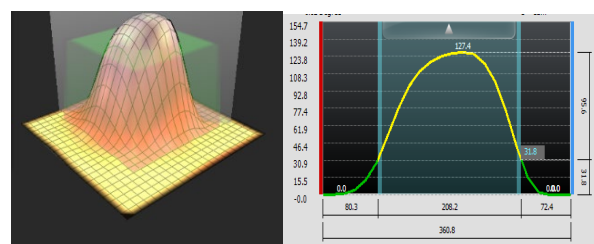


Figure 7. 3D images of Paste A print deposits on the Pad ID4516 printed on the **Printer 2**.

After printing, all boards were examined using high-end solder paste inspection system (SPI). Solder paste volume, average height and print area were measured. From the height measurements, the metric Delta H was used to quantify co-planarity across the device footprint. In order to optimize the entire surface mount process with mixed size components and presence of small apertures and larger thermal pads on BTC components, 3D imaging of the larger pads (**Figure 8**) was taken to document any printing defects (especially scooping).

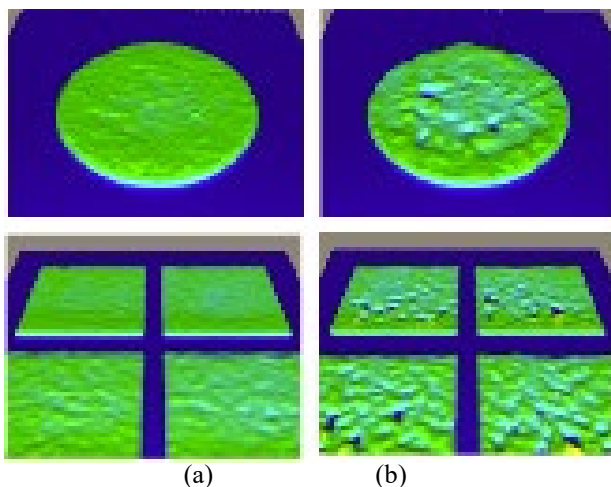


Figure 8. 3D images of the print deposits for Paste A printed on the thermal pads (a) 45 degree blade angle and (b) 60 degree blade angle

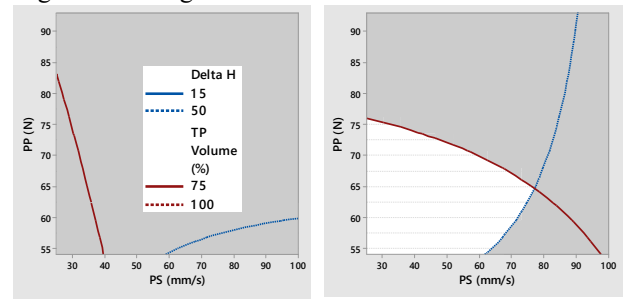
The measured response data was entered into Minitab software and an optimization analysis was done with the aim of maximizing the solder paste volume delivered to the pads, while minimizing co-planarity variation across the device footprint as captured by the Delta H value.

$$\text{Delta H} = \text{Max. Av. height of lead deposit} - \text{Av. height of thermal pad deposit}$$

Contour plots were generated from this optimization analysis for QFN and BGA components, at both 45 and 60 degree squeegee blade angles. The QFN contour plots show unshaded regions where the print parameters (print speed (PS) and print pressure (PP)) meet the criteria for greater than 75% solder paste volume on the thermal pad and less than 50 um Delta H. The BGA contour plots show unshaded regions where the print parameters meet the criteria for greater than 75% solder paste volume and a coefficient of variation (for volumes) less than 10%. The shaded regions in these charts represent print parameter settings that did not meet the required criteria. The contour plots for QFN components (U5 and U6) and Ball Grid Array (BGA) components (BGA144 and PBGA676) are presented below.

Based on the DOE results, it could be concluded that the new generation solder paste has a wider process window when compared to the old generation solder paste, especially with a 45° squeegee blade angle. The combined

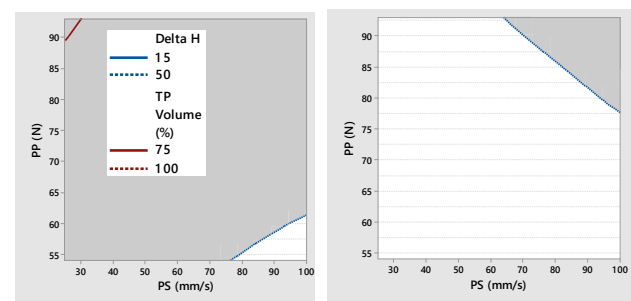
data for all QFN components shown in **Figure 17** demonstrates that the new generation solder paste has a wide operating window and can perform well with a 60 degree blade angle.



Old paste

New paste

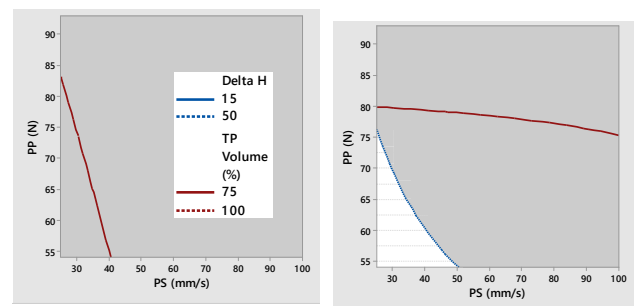
Figure 9. U5 component. Contour plot of Delta H for solder paste printed at 60 degree blade angle.



Old paste

New paste

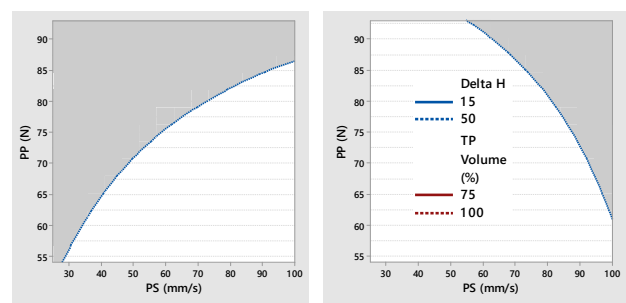
Figure 10. U5 component. Contour plot of Delta H for solder paste printed at 45 degree blade angle



Old paste

New paste

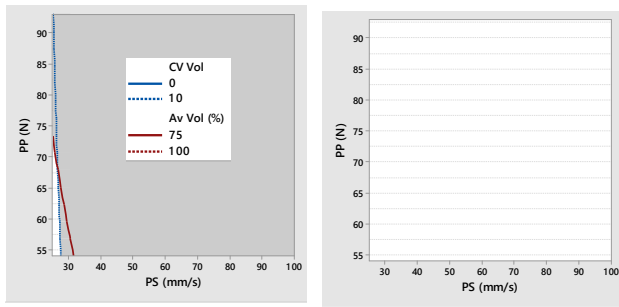
Figure 11. U6 component. Contour plot of Delta H for solder paste printed at 60 degree blade angle



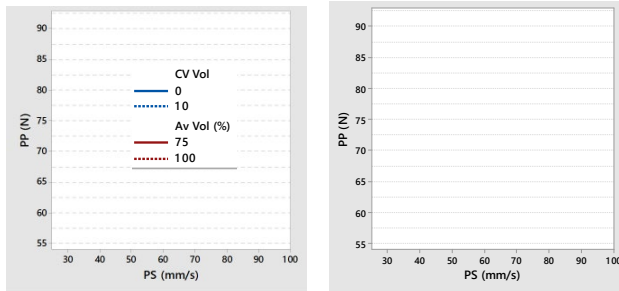
Old paste

New paste

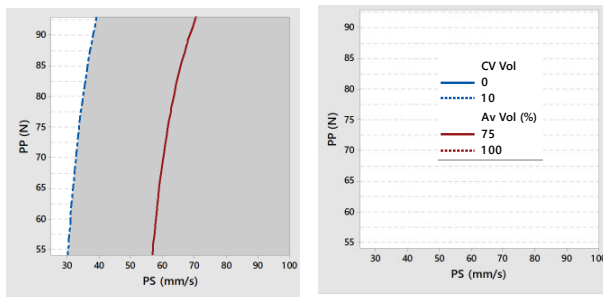
Figure 12. U6 component. Contour plot of Delta H for solder paste printed at 45 degree blade angle



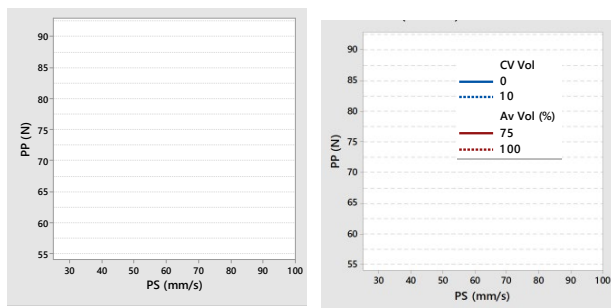
Old paste New paste
Figure 13. BGA144 (AR=0.54) Contour plot of Delta H for solder paste printed at 60 degree blade angle



Old paste New paste
Figure 14. BGA144 (AR=0.54) Contour plot of Delta H for solder paste printed at 45 degree blade angle



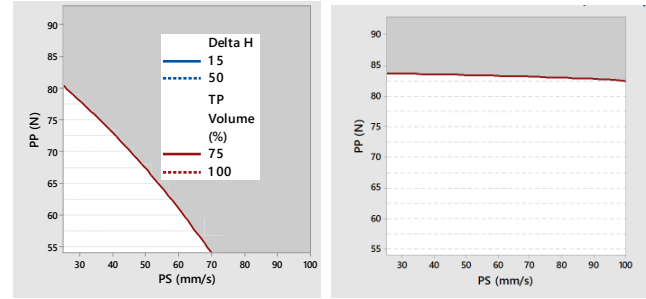
Old paste New paste
Figure 15. PBGA676 (AR=0.63). Contour plot of Delta H for solder paste printed at 60-degree blade angle



Old paste New paste
Figure 16. PBGA676 (AR=0.63). Contour plot of Delta H for solder paste printed at 45 degree blade angle.

A soak profile that meets IPC standards was chosen and used to reflow test boards printed using known good parameters from our optimization study. All the thermal pads on the test board were printed with a full pad design

with 90% pad area coverage. The voiding results for two QFN devices; MLF100 and MLF52, are shown in **Figure 18** and representative X-ray images in **Figure 19&20**.



Old paste New paste
Figure 17. Data for all QFN components contour plot of Delta H for solder pastes printed at 60 degree blade angle

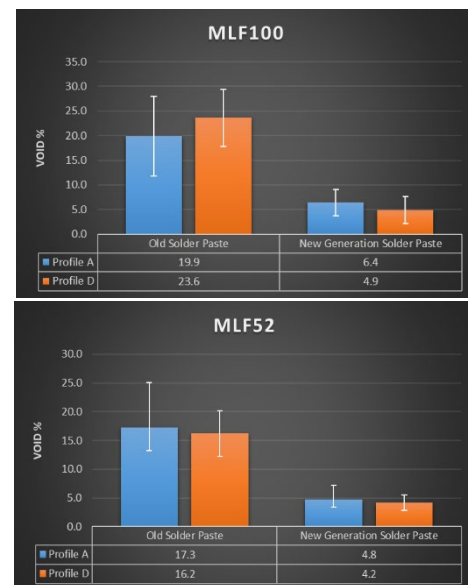
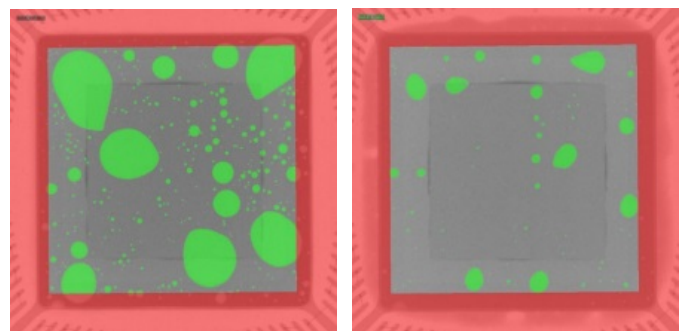


Figure 18. Voiding analysis for MLF100 and MLF52 components.

They show that the new generation solder paste produced a lot less voiding compared to the older generation paste irrespective of the proles used.



Old paste New paste
Figure 19. X-Ray images of MLF100 component

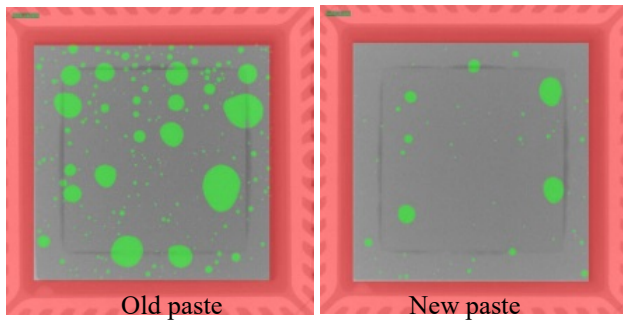


Figure 20. X-Ray images of MLF52 component

SUMMARY AND CONCLUSIONS.

A new generation of solder paste has been developed to specifically target BTC assembly challenges in particular voiding and solder print consistency. This study investigated the effect of paste rheology, print blade angle, and print process settings on the height consistency of print deposits for large and small features.

The most important finding is that older formulations of solder paste may not be effective at printing the large center terminations and perimeter signal terminations found on many BTC devices, with respect to the deviation in height of large center features and small signal features. The new generation solder paste tested in this study, with improved rheology, was capable of printing with good volume performance and good height consistency under a variety of process settings.

The most significant process setting was the use of a 45° blade angle. This enabled a very large window of print settings that provide low height deviations across large and small features simultaneously when used with the new generation solder paste. This also enabled height consistency with the old generation paste under a smaller set of conditions, where a 60° blade angle demonstrated an inability to meet the same level of height consistency.

The new generation solder paste was not only capable of meeting the printing challenges posed by having QFN components on an assembly along with a mix of other fine feature devices, but it also gave very good thermal pad voiding results as well.

ACKNOWLEDGEMENT

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