As originally published in the SMTA International Conference Proceedings.

NEW SOLDER BUMPING TECHNOLOGY AND ADAPTED ASSEMBLY PROCESSES FOR 100 µm PITCH FLIP-CHIP-TECHNOLOGY USING CAPILLARY FLOW OR NO FLOW UNDERFILL

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ABSTRACT
In this paper we will present new cost-efficient solder bumping and adapted assembly technologies for the processing of flip-chips with a pitch of 100 µm or less and solder ball diameters of 60 µm or 50 µm, respectively. The wafer bumping has been realized using a highly efficient Wafer Level Solder Sphere Transfer (WLSST) process. This technology uses a patterned vacuum plate in order to simultaneously pick up all of the preformed solder spheres, optically inspect for yield, and then transfer them to the wafer at once. This paper will discuss this technology and the process parameters for producing fine pitch solder bumps. The flip-chips were assembled on special BT- and FR4-material using reflow soldering. Due to the large thermal expansion mismatch between substrate and chip, special epoxy based underfill has to be used in order to increase the long term reliability of the lead-free solder joints. The use of capillary flow as well as of no flow underfill and applicable design rules for these highly miniaturized structures will be discussed. For cost efficiency reasons all processes investigated base upon standard processes of the surface mount technology, but are adapted to the requirements of highly miniaturized components. Results of the reliability tests will be discussed additionally. An analysis of the failure mechanism will be given and recommendations for further miniaturizations will be presented.

Key words: flip-chip, underfill, bumping, adapted assembly processes.

INTRODUCTION

The miniaturization of electronic packages is driven by a large variety of applications with high requirements on the level of integration and the form factor. This will be conducive to higher I/O-counts and a reduction of the pitch, which has an effect on the production systems as well. Due to size reduction and cost saving potential, flip-chip-technology has gained importance in the field of highly miniaturized electronic devices. Specific bumping processes have been established in recent years. Common methods for applying solder onto the semiconductor wafer are for example stencil printing, electroplating, solder jetting and controlled collapse chip connection new process (C4NP) [1]. The most important requirements for bumping are a high yielded, fast and cost efficient process as well as, in many cases, low tooling costs.

Bumping Technology

The stencil printing process is still the technology of choice due to the economical advantages by using pre-existing printing equipment in SMT production. With standard laser cut steel and nickel electroformed stencils peripheral arrays with 120 µm pitch can be printed at production level [2]. [3] has shown the wafer level stencil printing for 60 µm pitch using special nano-coated

stencils and type six and eight solder paste. With the nano-treatment of the side-walls and the bottom of the down to 20 µm thick stencils, the paste release from even very fine apertures can be improved.

The electroplating process is commonly used for high bump counts per wafer. The wafer is structured using a photolithographic process, which is followed by plating a copper mini bump on the bump sites. In a second photo patterning and plating process the solder alloy is applied and reflowed to form a sphere. With this technique, pitches down to 50 µm can be realized [4]. Due to the complex processes and mask manufacturing, the electroplating bumping technology is very expensive, especially for small wafer quantities.

Solder jetting is considered a very flexible bumping technology that is usable for three dimensional packaging, too. The process is flux-less and has additionally low thermal and mechanical stress input on the processed components. Solder ball diameters of down to 40 µm and a large variety of solder alloys can be used [5-6].

Very fine pitches down to 50 µm can be realized with the Controlled Collapse Chip Connection New Process (C4NP) which is described in [7-8]. According to a developed cost model, the C4NP process emerges lower cost compared to electroplating and stencil printing. The most critical cost factor of the C4NP process is the use of molds, since these impact directly the per wafer bumping costs.

All of the above mentioned bumping technologies require soldering or bonding technologies through conductive adhesives during assembly of the flip-chips. A new way for interconnects between component and substrate is described in [9]: The electrical connection is performed by the insertion of metallic pins in a ductile substrate material. With this special technology, a 30 µm pitch can be realized.

Flip-Chip Assembly

Besides the necessity of manufacturing very fine pitched bumps in order to cope with steady miniaturization, the production processes for assembling the flip-chips onto the substrates were improved as well. Circuitry structures that are eligible to the pitch of the dies were only realizable with thin film technology, which is very cost-intensive. Assembly machines used in high throughput production lines have to meet the needed placement accuracy as well and the vision systems have to detect the highly miniaturized bumps with high reliability.

Due to the heterogeneous material mix of the silicon die, the solder and the (anorganic) substrate material, a large CTE mismatch is inevitable. In order to absorb the thermal stress induced into the solder joints, underfill is used. The underfill technology can be divided into capillary flow and no flow processes. With capillary flow, the epoxy is applied after reflow soldering. The underfill flows underneath the die using the capillary effect. The flow rate and homogeneity of the underfill process is highly dependent on the gap size, the filler particle size, and the existence of residues of flux from the reflow process [10-11]. When using no flow underfill, a certain volume of the polymer based encapsulant is applied before flip-chip placement. After assembly, the solder is reflowed and the underfill cured during the same process [12-14].

Reliability Issues

One of the main reliability concerns in the flip-chip technology when using the highly miniaturized components on substrate level is the large mismatch of the coefficient of thermal expansion (CTE) between silicon die and printed circuit board. This thermal mismatch causes stress/strain in the solder joints. Various studies on solder joint reliability describe in detail simulation models and practical experiments. According to [15-16], the solder joint geometry has a highly significant influence on long term stability of the interconnections. Important parameters are the stand-off height and the contact angles of the solder joints on die and substrate side. To equalize the large thermal expansion mismatch, underfill materials is used in order to improve the reliability of the interconnections. Although some of the already mentioned influencing factors become less significant if underfill is applied, new possible influences appear, for instance the size of voids in the underfill [17]. In summary, the key factors that influence the long term reliability of the interconnections are named in [18]: The geometry of the solder joint, the underfill material, and the dimensions and the layout of the die.

As described in the paragraphs above, a large variety of solder bumping processes and assembly technologies have been established for the processing of flip-chips, of which each of the technologies has its own strength. In the following, this paper will present the technological enhancements of the Wafer Level Solder Sphere Transfer Technology (WLSST) for solder spheres of 60 µm and 50 µm in diameter and the assembly of test flip-chips on standard FR4- and BT-substrate materials using standard and modified SMT equipment and providing therefore a highly cost efficient process.

AIM AND PROCESSES USED

The aim of the experimental study presented in this paper was the bumping of flip-chips with 100 µm pitch and solder spheres of 60 µm or 50 µm, respectively, in diameter, the structuring of FR4- and BT-substrates with the necessary fine pitch structures, and the assembly of the dies using standard production equipment. This makes the process chain from wafer bumping to flip-chip assembly very cost efficient and flexible.

Wafer Bumping Process

The wafer bumping has been realized using the highly efficient and flexible wafer level solder sphere transfer process, also known as gang ball placement, that is described in detail in [1,19]. The WLSST tool can integrate several of the most necessary operations when depositing solder volumes on wafer level, like flux coating, solder reflow, inspection and rework processes, but can be configured to expand and complement the existing equipment and processes in the fab.

The main process steps of the bumping technology are shown in figure 1. Characteristic for this process is that all preformed solder spheres needed for one wafer are transferred to the wafer in one single process step. This is realized with a patterned vacuum stencil with openings corresponding to the under bump metallization on the wafer. The tool is placed over and lowered down to the sphere reservoir (a). Next vacuum is applied to selectively pick up the solder spheres. After inspection for missing (b) and extra (c) spheres the tool is aligned to the wafer. By lowering the stencil to the wafer the solder spheres are brought in contact with the wafer (d) on which flux has been pre applied. The process ends with turning off the vacuum and raising the tool (e) and reflow of the solder spheres (f). As yet with this technology it was possible to place solder spheres of 80 µm in size with high yields. For the research on the placement of 60 µm and 50 µm solder spheres the process in principle was not modified since the placement accuracy for tool to wafer of 15 µm is sufficient. By this the equipment can be still considered a standard process for wafer bumping.

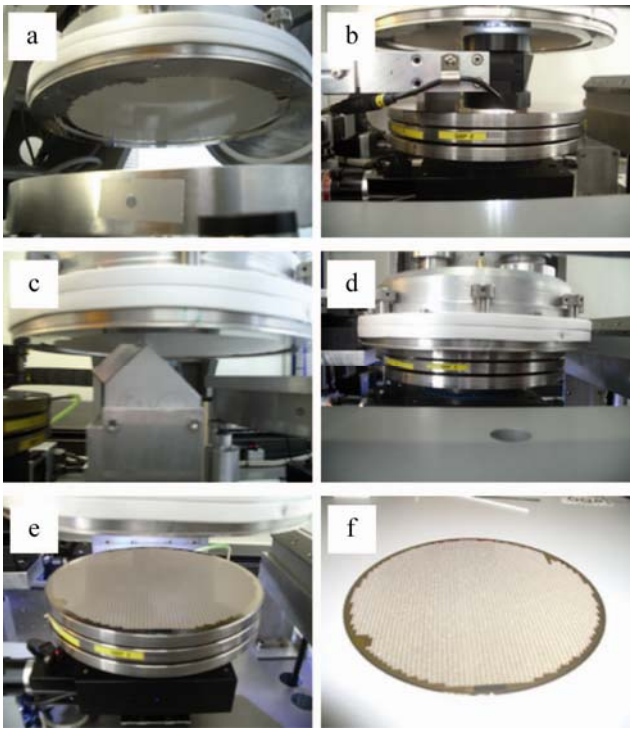


Figure 1. Process for wafer level solder sphere transfer technology

Stencils used in the WLSST technology can be manufactured similar to tools used for stencil printing technology. But for the placement of 60 µm and 50 µm predominantly the stencil quality had to be improved to secure sphere pick up and release. Laser cut stencils were compared to nickel plated ones regarding dimensional accuracy and achievable yield. The experiments showed that for high I/O-counts nickel plated stencils showed a better performance. The size of the openings should be slightly smaller than the size of the solder spheres. In case of the 60 µm solder spheres the openings had a size of 40 µm*40 µm. However, stencil thickness has only little influence on the process.

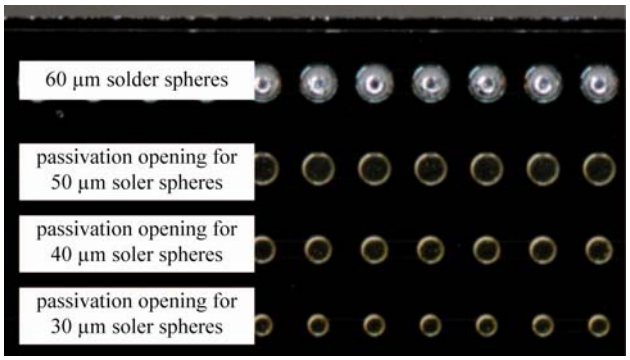


Figure 2. Chip with 60 micron solder spheres at the first row

The important parameters of the flip-chips used for the processability study presented in this paper are given in table 1. The silicon die has a thickness of 0.8 mm and an edge length of 10 mm. The preformed solder spheres are made of a SnAgCu alloy and are placed on a NiAu UBM realized in an electroless nickel process. Four rows of bumps have been realised at each side of the die, each with a different passivation opening for solder spheres measuring between 60 µm (first row) and 30 µm (fourth row) (figure 2). The I/O-count is dependent on the solder sphere size – for example 376 I/Os for 60 µm spheres, 368 I/Os for 50 µm spheres. 277 dies are placed on one wafer making it per wafer 104,152 I/Os or 101,936 I/Os, respectively for 60 µm spheres or 50 µm spheres, respectively. To detect failures during the reliability tests each die has a daisy chain structure.

Table 1. Parameters of the flip-chip

Flip-Chip		
Die Thickness		0.8 mm
Die Size		10 mm by 10 mm
UBM		NiAu
Solder Alloy		SnAgCu
Bump Count Chip/Wafer	60 µm	376/104,152
	50 µm	368/101,936
Bump Array		peripheral
Daisy Chain		Yes
Dies per Wafer		277

Layout and Substrate Structuring

It was the aim for the substrate structuring that standard and low cost processes can be used. The properties of the employed substrate materials are shown in table 2. The thickness of both materials is 0.8 mm. The coefficients of thermal expansion are nearly the same, whereas the glass transition temperatures varies about 30 K. The copper metallisation has a thickness of 9 µm at the beginning of the structuring process. After structuring and application of the solder mask, a NiAu surface finish was applied to the copper circuitry.

Table 2. Properties of the substrate materials

Substrate Material		BT	FR 4
Thickness		0.8 mm	
Glass Transition Temperature		210 °C (DMA)	170-180 °C (DSC)
CTE (<T_g)	x	15 ppm/K	17 ppm/K
	y	15 ppm/K	13 ppm/K
	z	55 ppm/K	55 ppm/K
Metallization		Cu - 9 µm	
Surface Finish		Ni/Au - 5-8 µm/50-120 nm	

The layout of the used test coupons is shown in figure 3. A number of six flip-chips can be assembled onto the substrate, whereas the structures of the flip-chip and the test coupon are realized in a way that only one layout is used for both, the dies with 60 µm and 50 µm spheres. Again, a daisy chain connection is integrated for each of the flip-chips and each chip can be connected for online measuring during reliability testing.

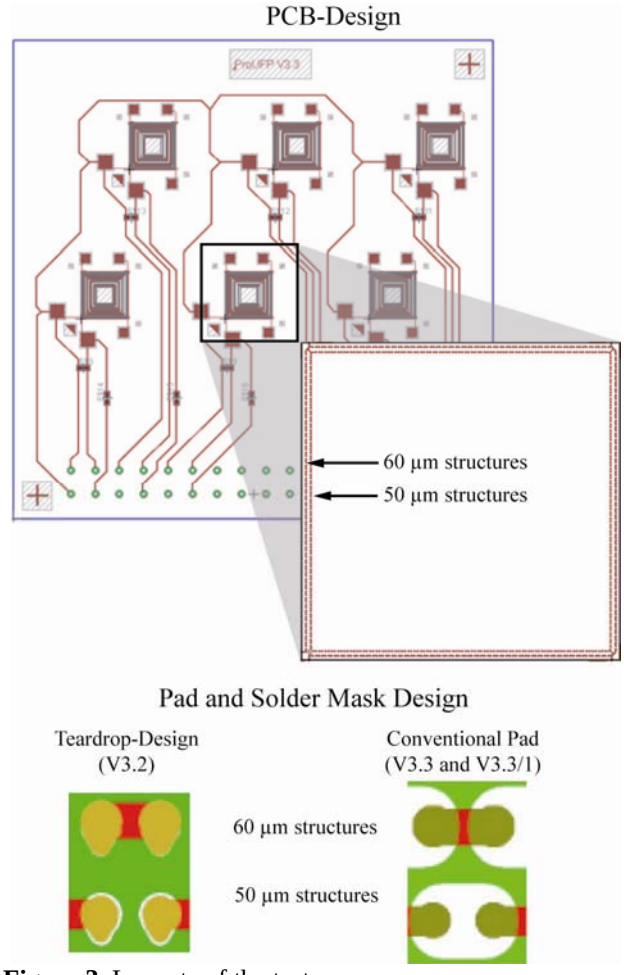


Figure 3. Layouts of the test coupons

The specification for the structures on the test coupon in terms of fineness were 40 µm lines and 50 µm spaces for the 50 µm solder spheres and 50 µm lines and 40 µm spaces for the 60 µm solder spheres. Additionally, two different foot prints were realized: One conventional design (V3.3 and V3.3/1) and one teardrop-design (V3.2) (figure 3), whereas V3.3/1 is an improved version of V3.3 concerning solder mask registration. A preliminary test showed a very good wetting of the solder spheres on the land pads. Therefore, against usual procedure, ultra fine pitch solder mask defined pads were realized as well on the test coupons.

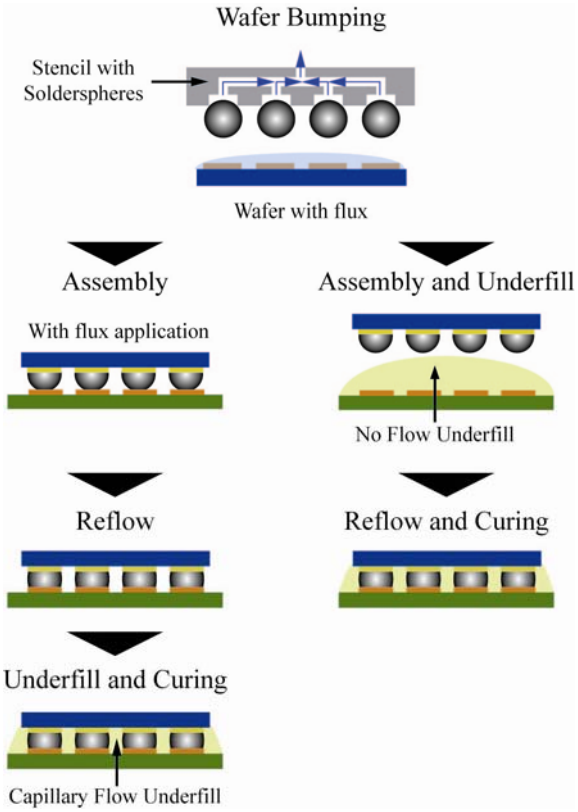


Figure 4. Investigated assembly processes: Capillary Flow Underfill (left) and No Flow Underfill (right)

Table 3. Parameters of the assembly process

Assembly Process	
Production Equipment	Die bonder, forced convection soldering oven, dispensing equipment, work piece carrier
Capillary Flow Underfill	A, B
No Flow Underfill	Q, P

Assembly Process and Reliability Testing

The processes used for the assembly of the components on the test coupons were carried out on standard production equipment (table 3). Two separated process chains were investigated for the assembly of the flip-chip with 60 µm and 50 µm solder bumps (see figure 4). One was the classic process with capillary flow underfill. Flux was applied to the substrate right before component placement. After forced convection reflow soldering, the underfill was dispensed in L-shape. Two different underfills were in use. Throughout all process steps the test coupons were attached to a work piece carrier in order to minimize the bending of the substrates during die placement and reflow soldering. The second process investigated is the use of no flow underfill. Before

component placement a defined amount of underfill was dispensed Dot- or X-Shape, respectively. Two no flow underfills have been used. Subsequently, the die was assembled with varying placement velocities, placement forces and holding times after placement. During reflow soldering the solder wets the land pads and the underfill cures. A work piece carrier has been used during this process chain as well.

Table 4. Test program for assembly tests (capillary flow underfill)

Exp. No.	Test Coupon	Solder Sphere	Row on Flip chip	Under-fill
1	3.2	60 µm	1st row	B
2	3.3	60 µm	2nd row	B
3	3.3/1	60 µm	2nd row	B
4	3.2	50 µm	2nd row	A
5	3.2	60 µm	1st row	A

For the experiments with capillary flow underfill, the combination of solder sphere size, passivation opening and footprint diameter has been varied in several iterations.

In the first version the passivation opening and the footprint were of the same size. For experiments number 2 and 3 the 60 µm solder spheres were placed on the 2nd bump row during wafer bumping (see figure 2) to increase the stand-off after reflow soldering and therefore increasing the long term reliability of the solder joints. The difference lies in the PCB layout, since V3.3/1 is an improved version of V3.3. For experiments 1 to 3 underfill B has been used. In version 4 and 5 the passivation opening and the footprint were of the same size. Aim of this experiment was the comparison of the reliability of the solder joints formed of 60 µm or 50 µm solder spheres, respectively. Experiments 4 and 5 were carried out using underfill A.

Table 5. Test methods for reliability testing (capillary flow underfill)

Reliability Testing		
No. 1	DIN EN 60 068-2-14	1,000 Cycles -40 °C/+125 °C
No. 2	MIL-STD883G, Method 1010.7, Condition B	4,000 Cycles -55 °C/+125 °C
No. 3	EIA/JESD22-A101-B	85 % rel. humidity 85 °C 3 V

Different methods of reliability tests have been carried out with the test coupons (table 5). The test coupons from experiments 1 to 3 were tested according to MIL-STD883G, Method 1010.7, Condition B (-55 °C/ +125 °C). Humidity testing was carried out as well according to EIA/JESD22-A101-B. The specimen of experiments 4 and 5 were stressed 1,000 cycles -40 °C/ +125 °C according to DIN EN 60 068-2-14. All specimens were connected to an online measuring system in order to determine the exact cycle of the first failure.

	60 µm Bump	50 µm Bump
Average Height	44.8 µm	36.3 µm
Standard Deviation	0.5 µm	0.7 µm
Average Diameter	66.5 µm	61.8 µm
Standard Deviation	0.8 µm	0.9 µm

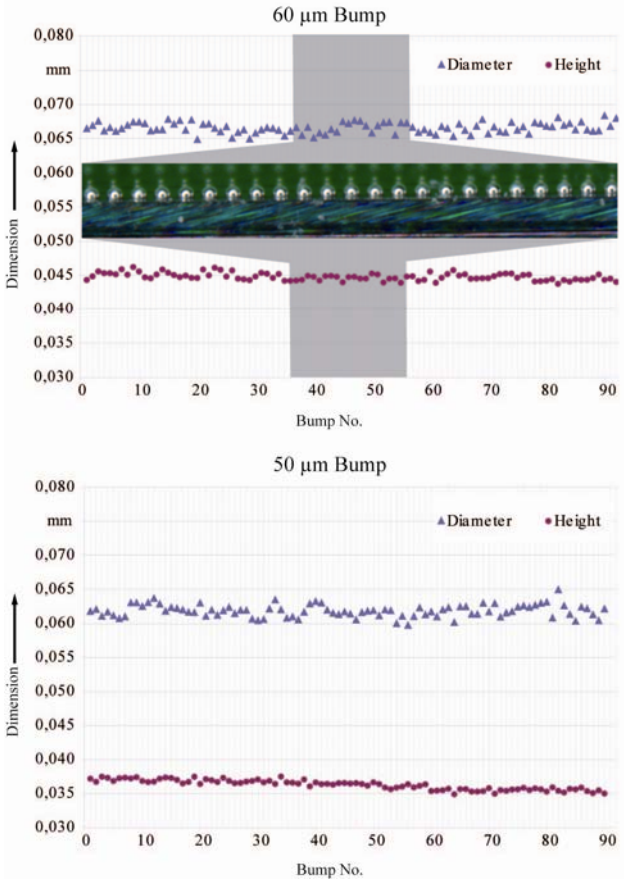


Figure 5. Measurement of height and diameter of 60 µm and 50 µm solder spheres, respectively

RESULTS AND DATA OBTAINED

Wafer Bumping Process

For the wafer bumping process, the yield is of highest importance. With WLSST technology, 60 µm solder spheres can be placed with a yield of 99.8 % per Wafer. A uniform height and diameter of the bumps on the flip-chip are very relevant for the following process steps and especially have an influence on the reliability of the solder joints. Therefore the height and diameter of the solder bumps have been measured using a Werth Videocheck IP 400HA system. Exemplary the results for one side of a chip is shown for 60 µm and 50 µm solder spheres. As can be seen a sphere diameter of 60 µm results an average bump diameter of 66.5 µm (standard deviation: 0.8 µm) and an average height of 44.8 µm (standard deviation: 0.5 µm). Accordingly, a 50 µm solder sphere in initial state results a solder bump with an average diameter of

61.8 µm (standard deviation: 0.9 µm) and an average height of 36.3 µm (standard deviation: 0.7 µm). This shows that for both, the 60 µm and the 50 µm solder spheres very uniform solder bumps can be achieved on the flip-chip.

Layout and Substrate Structuring

To improve the yield during assembly and underfill of the flip-chips, several improvements on the structuring of the metallization and the solder mask of the test coupons have been made. As described before preliminary tests have shown that a solder mask is absolutely essential for high yields after reflow. The quality of the metallization is shown in figure 6. As can be seen very precise structures could be realized on both the FR4 and BT substrates. Even ultra fine pitched structures with lines of 20 µm are of high accuracy.

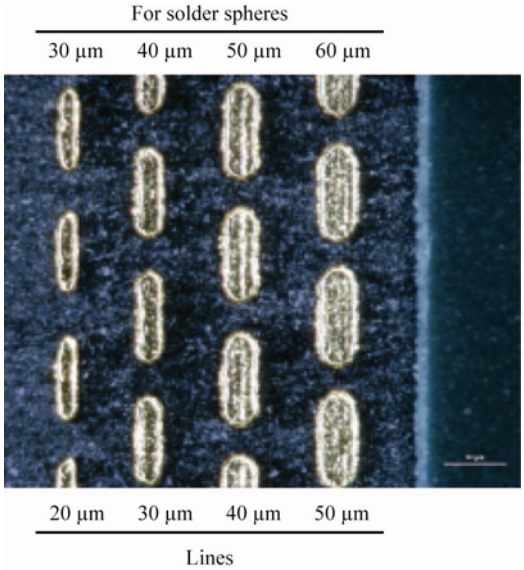


Figure 6. Quality of the ultra fine pitch structures (Layout V3.3 before solder mask application)

Regarding the solder mask quality the registration to the metallization, the height of the mask and the web width are of highest importance. All have direct influence on the long term reliability of the solder joints. A precise registration and web widths are needed for uniform footprints. A solder mask height as small as possible reduces the gap between the mask and the bottom side of the flip-chip what enhances the flow of the underfill.

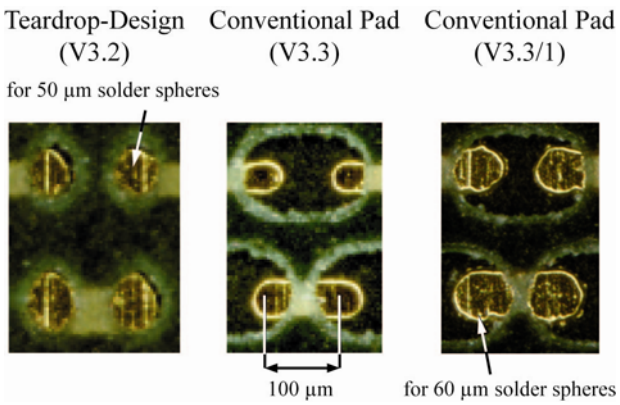


Figure 7. Accuracy of pad and solder mask

Two different foot prints and solder mask openings have been realized. On the one hand a tear drop design to support x-ray inspection (V3.2), on the other hand a conventional design to form solder joints as constant as possible (V3.3 and V3.3/1). Both designs show very good registration as can be seen in figure 7.

The dimensions of the metallization and the solder mask are shown in figure 8 in a cross section view for the 60 µm structures. The structuring of the metallization results in a line width of 46.7 µm (nominal 50 µm) and a height of 9.4 µm. Solder mask height is 25 µm.

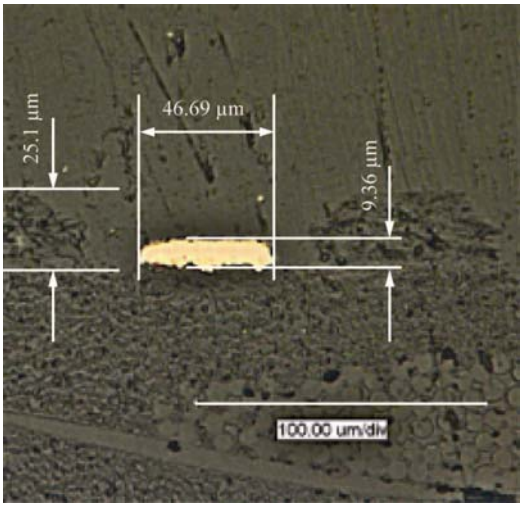


Figure 8. Cross section view of the metallization (60 µm structures) and the solder mask opening (V3.3)

Assembly Process

For flip-chip assembly the production yield is of high importance as well. Therefore the functionality of the assembled dies was tested after reflow and underfill, respectively table 6. On the layout with the teardrop design (V3.2) a yield of 89.6 % for the flip-chips with 60 µm solder bumps and 81,3 % for the dies with 50 µm solder bumps could be achieved. Although the yield is quite good, a better yield is limited to the tolerances in the solder mask. For theses highly miniaturized structures it is essential that the registration of the solder mask fits precisely to the metallization. And even though the solder mask registration shows only tolerances of a few microns the yield suffers from the very fine structures of the solder mask in layout V3.2.

Table 6. Comparisons of the yield after reflow (capillary flow underfill process)

Experiment No. (test coupon, solder sphere, row on Flip chip)		Yield (after reflow)
1/4	(V3.2, 60 µm, 1st row)	89,6 %
2	(V3.3, 60 µm, 2nd row)	93.1 %
3	(V3.3/1, 60 µm, 2nd row)	100 %
5	(V3.2, 50 µm, 2nd row)	81.3 %

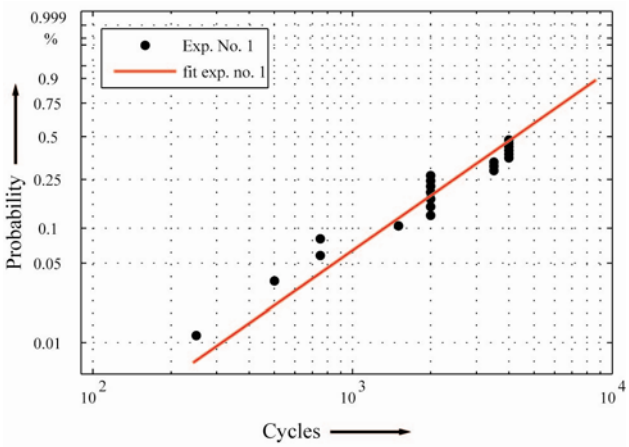
If the openings in the solder mask are increased, the tolerance of the registration of the solder mask to the metallization becomes less critical. With layout V3.3, the

yield could be raised to 93.1 %. With an improved printed board version (V3.3/1), a yield after reflow of 100 % has been achieved in fully automated assembly of the flip-chips.

As yet in the no flow underfill process a yield of 57 % could be achieved with underfill A on the layout v3.3. As the research is still underway even better yields can be expected, especially with the improved layout V3.3/1.

Reliability Testing

The reliability testing of the test coupons of experiment 1 are carried out according to MIL-STD883G, Method 1010.7, Condition B and EIA/JESD22-A101-B. Figure 9 shows the Weibull plot for printed board version 3.2 with chips with 60 micron solder spheres at the first row. The capillary flow underfill B has been used for these experiments. As can be seen 51 % of the dies show still no failure after 4000 cycles. With this result, a characteristic life of 5,285 cycles can be calculated using the maximum likelihood method. The form factor of 1.16 indicates a process in steady state. But 24 % of all failures on the tested coupons occur before 1,500 cycles and can be considered early failures. The reason for those early failures could be traced back to the very small openings of the solder mask of layout V3.2. The slightest variation from the nominal dimension of the opening leads to a solder joint of irregular shape. This again leads to an uneven strain distribution in the solder joint causing an early failure.

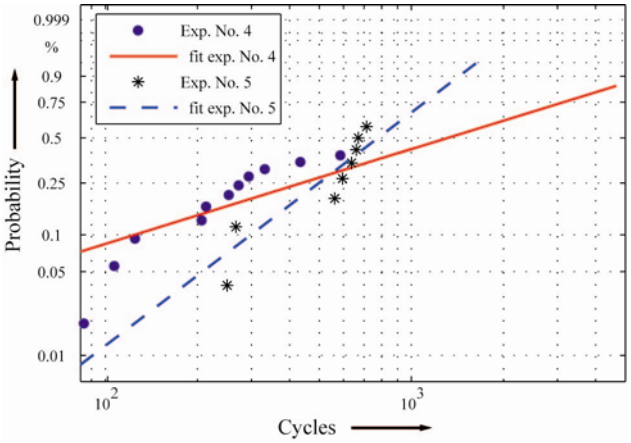


Exp. No.	Characteristic Life α	Form Factor β
1	5,285 cycles	1.62

Figure 9. Weibull plot for printed board version 3.2 with chips with 60 micron solder spheres at the first row (experiment no. 1)

The reliability tests with printed boards from experiment 2 and 3 are still in progress. According to the present knowledge from the results of the tests a similar reliability of the solder joints can be expected.

The reliability testing of the test coupons from experiment 4 and 5 (underfill A) was carried out according to DIN EN 60 068-2-14. One thousand cycles were performed. Figure 11 shows the Weibull plot for those experiments. The calculated characteristic life of the components is 2,067 cycles, what is still considered a good result for those extremely high miniaturized assemblies. As can be seen, over 70 % of the failures of the test coupons with 60 µm solder joints happen before 300 cycles. The assumption for the root cause of the early failures is supported by the form factor, which has a value of 0.8. The reason for that is described above and can again be traced back to the solder mask. This becomes obvious when looking at the results for the 50 µm solder spheres. For those even smaller structures in the solder mask even the slightest tolerances become critical in terms of the reliability of the solder joints. This leads to a relatively low characteristic life of 977 cycles. The form factor of 1.97 indicates that the defects are no early failures. But again, with the improved layout V3.3/1 notable better results are to be expected during life cycle testing.



Exp. No.	Characteristic Life α	Form Factor β
4	2,067 cycles	0.8
5	977 cycles	1.97

Figure 11. Weibull plot for the comparison between 60 µm and 50 µm solder spheres (experiments 4 and 5)

A characteristic sign for a failure of the flip-chip is shown in figure 12. During hold time at high and low temperature, respectively, the voltage increases and decreases slightly as can be clearly seen in the left side of the upper diagram in figure 12. Through this significant signal difference, the number of temperature cycles can be identified. The drop of the signal during temperature change indicates the beginning of a crack in the solder

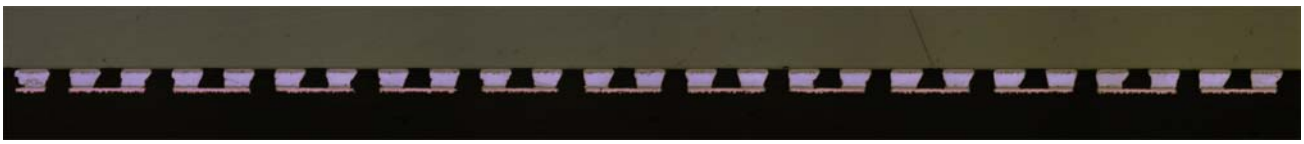


Figure 10. Cross section view of assembled flip-chip with 60 µm solder spheres

joint. After several drops the signal starts jittering at high temperatures, indicating crack growth. During the course of temperature cycling, the signal starts jittering at low temperatures as well, leading finally to a failure of the solder joint.

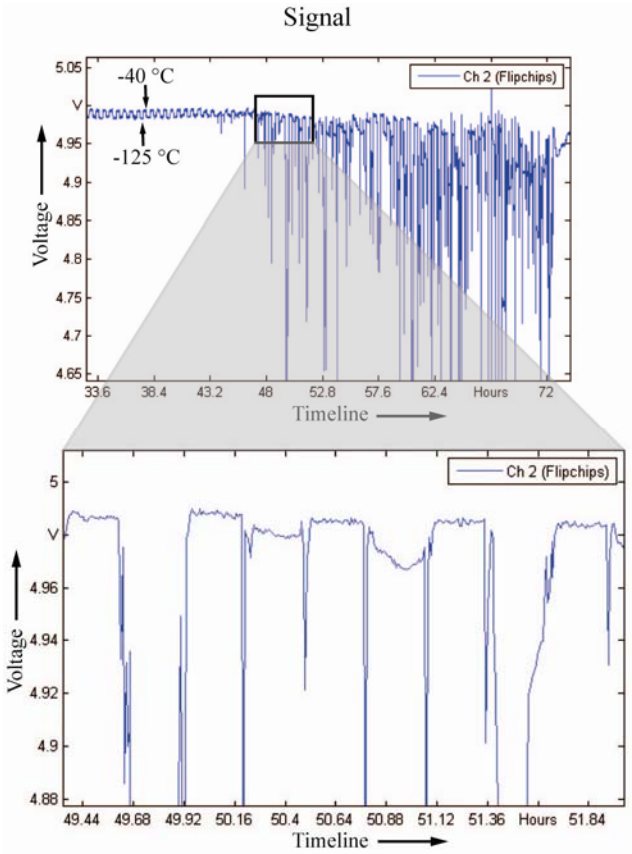


Figure 12. Signal from online measuring during temperature cycling

The Figures 10 and 13 show exemplary cross section views of the solder joints of test coupons with capillary flow underfill. The solder joint on the left of figure 13 shows a slight bend defined by the solder mask. Such an asymmetry can lead to accelerated cracking of the interconnection.

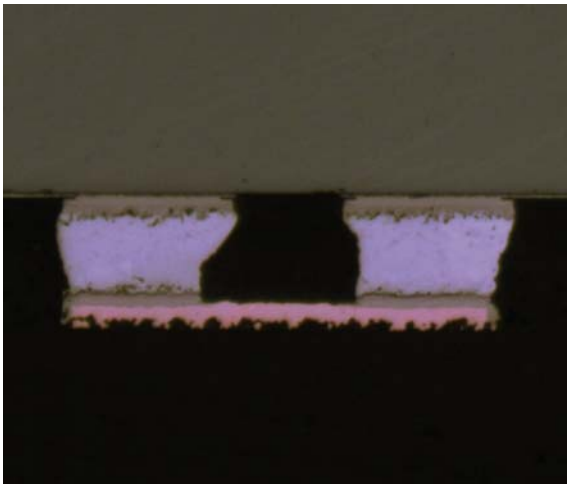


Figure 13. Cross section view of the solder joints

CONCLUSION

In conclusion, we have presented a new low-cost manufacturing technology for ultra fine pitch flip-chip applications based upon standard processes of the surface mount technology. Solder spheres with a diameter of 60 µm as well as 50 µm can be placed onto wafers simultaneously using the highly efficient and flexible wafer level solder sphere transfer process also known as gang ball placement with very high yield. The automatic assembly of the flip-chips has been demonstrated. The yield of the flip-chip process is depending from layout and tolerances of the printed boards, especially from solder mask registration and solder mask tolerances. With the final printed board layout we obtained 100 percent assembly yield (n=32) after underfill. The root cause for early failures during temperature cycling could be identified and will be conducive to improved reliability results using printed boards with the final layout. Underfill selection and underfill process optimization are crucial for the long term reliability of those extremely high miniaturized assemblies.

ACKNOWLEDGEMENTS

The authors would like to thank Mr. Thomas Friedrich from MSE for automatic assembly of the chips and Mr. Bernd Burger from MSE for cross sectioning several test coupons. The results presented in this paper have been achieved within the project *Process Technology and Connection Methods for Ultra Fine Pitch Components*. The authors would like to thank the Federal Ministry of Education and Research of Germany for funding under contract 02PG2361, 02PG2362, 02PG2363 and 02PG2366.

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