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THE QUEST FOR RELIABILITY STANDARDS

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ABSTRACT

As electronic assemblies become more complex each Original Equipment Manufacturer (OEM) struggles with the question as to whether the product will work in the intended environment, for the length of time expected by the user. Many methods have been developed to simulate the end-use characteristics of equipment in the field, but a clear understanding is required to differentiate between the methods used to assess quality and those used to validate reliability. The considerations and relationships between the customer and supplier are also now a major factor, especially since most OEMs outsource not only the fabrication, but also the design of the product.

The industry trade associations have written many standards which define methods for both quality conformance and reliability testing. Sometimes these methods are misapplied; however there should be no misunderstanding about the fact that poor quality can never achieve the intended reliability of the product. Quality conformance is meeting the requirements of the customer. Since each end-use varies classes or levels of complexity and performance were developed in most of the performance standards in order to simplify the procedures for determining whether the finished goods meet the customer requirements. There is no doubt that the requirements for a hand-held commercial product are different than those for an aerospace application. Also the degree of validation of both quality and reliability differs, as does the cost of producing the item.

Some of the existing reliability methods have become suspect in simulating the end-use, so some OEMs are requiring new methods in order to accept delivery of those products indicated in their fabrication documentation package. Reference to classes or levels of quality are not a guarantee that the product will perform according to its reliability assessment. An example is one where an OEM has developed a product and the prototype version has been tested to validate the reliability of the unit in its intended use. The production version is then outsourced to a new fabricator and it is unclear as to whether the new supplier's process is robust enough to achieve the same reliability as the original prototype.

The dilemma facing the industry is that the supply chain is hard pressed to keep up with all the new "home-grown" methods and new stress techniques being developed. The concepts badly need industry consensus on robustness and reliability assessment methods linked to the end-use environment. This paper explores the various alternatives.

BACKGROUND

The idea of testing a product in order to establish a form of reliability is not new. Many companies that manufacture products for use in the industry want to establish some form of verification that the product will work for the time expected by the customer. These tests have been developed in order to stress the product to the point where a determination can be made as to the products' ability to survive under extreme conditions. Highly Accelerated Life Testing (HALT) has been in existence for over 40 years. Based on the simple idea that if the product was tested beyond specifications the developer would better understand the design margins and improve the products' robustness in the field where it will be used.

Hewlett Packard started life testing in the early seventies. It was David Packard who believed that "Reliability cannot be achieved by adhering to detailed specifications. Reliability cannot be achieved by formula or by analysis. Some of these may help to some extent, but there is only one road to reliability. Build it, test it and fix the things that go wrong. Repeat the process until the desired reliability is achieved. It is a feedback process and there is no other way". Some think that the work of HP in the 70's was a predecessor to HALT testing.

A good combined definition for HALT is that it is a Design technique used to discover product weaknesses and improve design margins. The intent is to systematically subject a product to stress stimuli well beyond the expected field environments in order to determine and expand the operating and destruct limits of the product. As such many pieces of equipment have been developed that can provide these stresses which include cold temperature, hot temperature, rapid thermal transitions, vibration and shock stress, and combine thermal and vibrational environments. There is a similarity between Design for Robustness and HALT except that the latter is intended to take the product to failure during testing, understanding the failures, and improving the design of the product.

In order to expose the product to the HALT conditions requires that the entire product is subjected to the stresses intended to simulate the severity of the environments that might be encounter. In many instances many aspects of the product is able to survive the stresses, and the redesign normally concentrates on those aspects that are the subject of the failure. If the vibrational stresses caused the problem it is a simple matter to add mechanical structures to enhance the capability of the product to resist the impact of the vibration or shock. Thermal transitions however are a little more difficult to isolate especially if these are severe and cover a large range between hot and cold.

The Weakest Link

The electronic assembly within any container has always been the subject of reliability concern. Since the functions of the product would be severely impaired, some designers build redundancy into the electronics. If a circuit was going to fail an alternate would take over to accomplish the same task or to provide a warning to the user that something needed to be replaced or recharged or whatever it took to get the product to work correctly. These solutions were usually not sufficient in order to establish a high level of confidence by the customer.

Once the idea of using multilayered circuitry was established in the 1970s, the interconnection between layers was determined to be the weakest link of the electronic assembly. Electronic components were tested and after the assembly, were subjected to Burn-In exposure. If they passed these conditions their failure rate was minimized for a long period. Through-hole attachment and good solder joints provided sufficient mechanical strength to offset some of the vibrational stresses, and the thermal characteristics imposed on the assembly were not sufficiently detrimental to offset the pretesting accomplished by the component supplier to prove that the components would be reliable in many different environments.

The concern was for the plating in the plated-thru holes of the multilayer board. The only electrical connection made between the inner layers of circuitry was the plating that served to coat the inside of the hole. The process was one with multiple steps each of which could cause serious problems in performance within the field. After the assembly saw many thermal cycles of hot and cold, during the normal product operation, the concern was that the plating attached to a particular layer would come apart. In addition, with thousands of holes in any multilayer panel, or for that matter large backplane, it was not possible to examine and certify that each hole would survive the thermal stresses of normal assembly operation. The process needed to produce a reliable product.

Once the various layers had been prepared with their defined circuitry, they were laminated into a homogeneous structure. This effort was normally accomplished in a panel format with the individual boards outlined to be later sectionalized as they become separated boards or assemblies. The plated through-hole drilling was the most critical part of the process, and if not accomplished properly would eventually lead to product failure due to the following steps not accomplishing their goals of interconnection attachment. Drill speed and feed played a part, as did the number of times that a drill should be used. Drill wear was critical, and coupons used in the panel allowed the manufacturer to check the quality of the hole by drilling the coupon the first time the drill was used and then the last time.

Drills get hot, and as they remove material from the multilayer hole structure they are cutting through copper, glass reinforcement and resin; usually some form of epoxy. The heat of the drill causes some of the epoxy resin to be transferred to some of the copper at the ring intended to be connection to the barrel of the plated through hole. The term “Resin Smear” became a key element of the drilling process. How much was there? And how could it be removed before the plating was added to the inside of the hole? Some companies claimed that their drilling profiles did not produce any resin smear. Others used some chemistry or plasma gas etching to remove the excess resin in the hole. The National Security Administration (NSA) insisted that the holes needed to be etch-backed with sulfuric acid in order to remove some resin and glass and provide a three corner lock of the plated through hole as shown in Figure 1. And the reliability debate raged on for ten years.

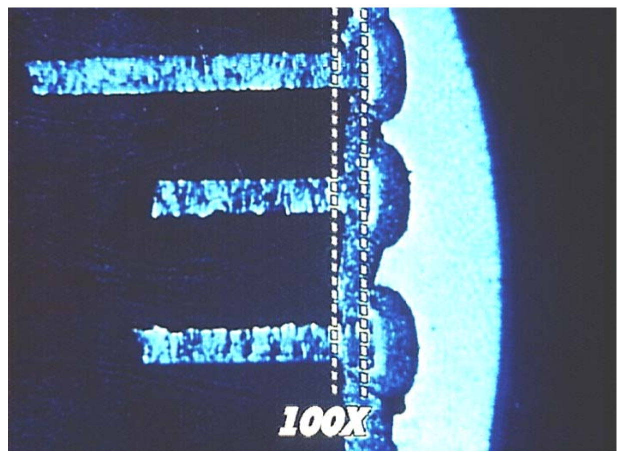
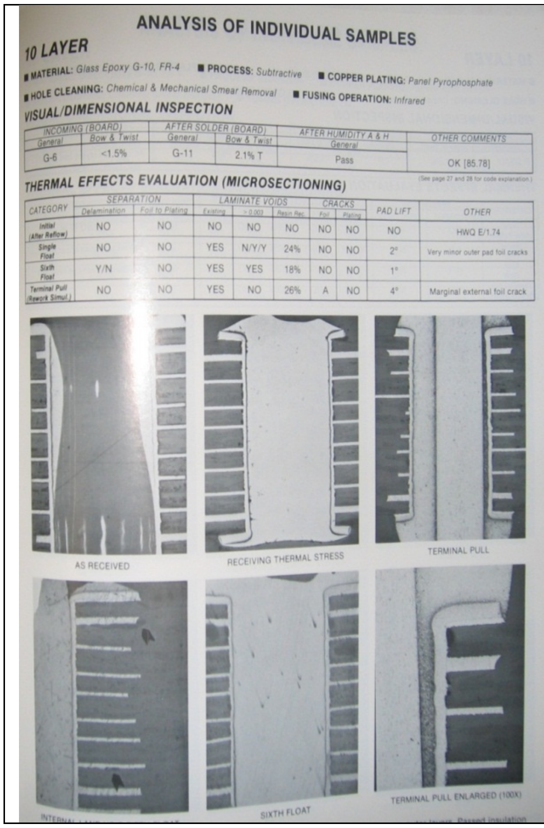


Figure 1 Plated-thru hole with etchback

The discussions on reliability took place in the multilayer committee of IPC. The only way to settle the issues was to perform a round robin test. The committee wrote a test plan, companies volunteered to build samples using and identifying their process, while others volunteered to stress the samples and prepare the final report. After Five Multilayer Round Robins what did the industry learn about hole de-smear and plating; etchback and non etchback? It appeared that if the process was good and there was no resin smear, or it was properly removed that the board circuitry would survive in the field. The effort was painful for the industry in order to establish plated thru hole quality requirements and how they related to reliability. Different plating cracks were identified and whether they promulgated or not. And techniques of using coupons on the panel were established as a measure of the quality of the plated through holes.

Figure 2 shows an example of a page from Multilayer Round Robin V which highlights the differences that were found in various samples. Not all the products submitted were acceptable and even then since the requirements for Commercial, Military and Hi-Reliability were different it became obvious that product would perform sufficiently in different environment due to the different stresses that were imposed by the environment. One needs to remember that the environment provides stress, but so does the processing of the product. As the industry learned over the years the products first sees the stresses imposed by the assembly process conditions. Some of these include the repair or modifications. Second are the environmental conditions imposed by the use the of the product such as a board mounted to the engine block of an automobile, and finally the normal component and circuit wear-out due to the on/off, hot/cold differentials. Much of this was learned as the industry did other round robins on small hole, or stress sequence evaluations.



ANALYSIS OF INDIVIDUAL SAMPLES

10 LAYER

■ MATERIAL: Glass Epoxy G-10, FR-4 ■ PROCESS: Subtractive ■ COPPER PLATING: Panel Pyrophosphate
■ HOLE CLEANING: Chemical & Mechanical Smear Removal ■ FUSING OPERATION: Infrared

VISUAL/DIMENSIONAL INSPECTION

INCOMING (BOARD)		AFTER SOLDER (BOARD)		AFTER HUMIDITY A & H	OTHER COMMENTS
General	Bow & Twist	General	Bow & Twist	General	
G-6	<1.5%	G-11	2.1% T	Pass	OK [85.78]

(See page 27 and 28 for code explanation.)

THERMAL EFFECTS EVALUATION (MICROSECTIONING)

CATEGORY	SEPARATION		LAMINATE VOIDS			CRACKS		PAD LIFT	OTHER
	Delamination	Foil to Plating	Existing	>0.003	Resin Rec.	Foil	Plating		
Initial (After Reflow)	NO	NO	NO	NO	NO	NO	NO	NO	HWQ E/1.74
Single Float	NO	NO	YES	N/Y/Y	24%	NO	NO	2°	Very minor outer pad foil cracks
Sixth Float	Y/N	NO	YES	YES	18%	NO	NO	1°	
Terminal Pull (Rework Simul.)	NO	NO	YES	NO	26%	A	NO	4°	Marginal external foil crack

Commercial

Military

High-Rel

Accept Conditions

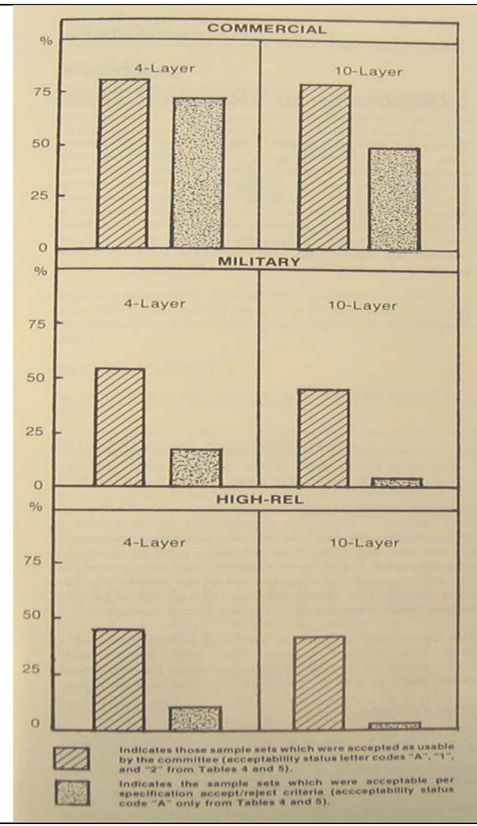


Figure 2 Sample pages from Multilayer RR V for Ten and Four layer Board Samples

It sometimes takes a long time for the industry to agree on a particular aspect when something unusual takes place. Just as all the work of the Multilayer Round robins was coming to closure during the coupon preparation someone noticed some dark spots near the inside of the plating of the hole. Identified as a sulfination void these dark spots were nicknamed "Resin Recession". It was explained that when the sample was floated in hot solder some of the resin which was not completely cured receded from the hole wall. When asked how much could be tolerated the military said none; while the industry said 100%. After 2 hours of discussion a compromise was reached that 40% resin recession was acceptable; while 41% and above was a reject. For the next five year the industry threw away panels where the coupons exhibited more the 40% resin recession.

At the end of the multilayer round robins it was decided to see what happened to the holes with examples of the black dots. Samples were solder-floated once, twice, three, four five and six times with no extra damage and all circuits still connected. Finally the "thermal zone" was established in the standards as shown in Figure 3. This zone is used to examine the plating integrity and no longer evaluates the resin. The industry continues to be paranoid about the reliability of the product as well as the quality used to make sure that the reliability can be achieved.

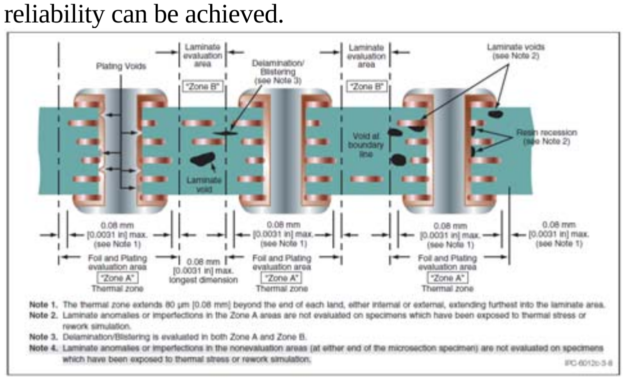


Figure 3 Coupon Examination to Determine Plated Through-hole Quality

SURFACE MOUNTING

With the move to surface mounting the industry faced new challenges on reliability. During that era many wondered if attaching parts to the surface of the conductive pattern would survive the stresses that an assembly would see. Not only was there concern about the solder acting as the only mechanical securing mechanism, there was also the possibility that the land pattern on the printed circuit board would tear away. Many tests were in existence that had been developed to assure copper foil adhesion. Some of these were peel strength while others dealt with hole plating pull-away. Never-the-less it was important to determine if the solder joint itself had sufficient strength to sustain the vibrational elements or bending moment of the mounting substrate that would stress the solder joint mechanical strength.

In the late 1980s four engineers from AT&T published a paper entitled "Surface Mount Solder Attachment Reliability Figures of Merit – "Design for Reliability Tools". This paper was presented as a part of the SMART conferences in January of 1989. By that time the engineers at AT&T had perfected the equations for determining the methodology for a good DFM model. They had proven the concepts by testing varies AT&T products to determine the possible failure mechanism based on the number of thermal cycles that the product would experience. Their concept consisted of four basic Figure of Merit (DF) equations starting with different components, whether they were leaded or leadless, and their size and expansion rate. The results were factored into the second equation which considered the mounting substrate and its expansion rate in the X & Y axis. Equation number 3 considered the upper and lower limits of the thermal characteristics to which the design would be exposed. The final equation into which the first three were factored considered the life cycle expectancy of the assembly. Essentially the concept considered:

- Determine the FM (comp) for all components in the design (these should be in the component catalog)
- Determine the FM(assy) for all components in the design based on the choice of substrate
- Determine the FM(env) for all components in the design based on the system thermal environment and component power dissipation
- Determine the FM(use) for all components in the design based on the expected product cycle life and the allowable failure probability
- Determine the FM(use) for the design from the lowest FM(use) for any of the components in the design provided the allowable failure probabilities were chosen to reflect the number of components and component mix in the design.

The final step in all the equations is the analysis that makes the determination as to whether the design meets reliability requirements. If the FM(use) was equal to 1 or greater the design was adequate; if the result of the four equations was 0.7 or less the design did not meet reliability requirements. Anything in between required some rethinking or contacting a reliability expert. The ideas of the AT&T work were discussed further by the SMT Accelerated Reliability Test Task Group and the focused on providing the industry with all the tools needed in order to establish good product that was reliable and by November 1992 they published the IPC-SM-785 "Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments.

The work of this committee did more than just publish a great standard they also provided the industry with a snap shoot of nine end-use environments as shown in Table 1. The concepts identified the minimum and maximum temperature as well as the average range between the upper and lower limits in any use case; the number of hours between on/off that the product would operate each day and the number of cycles each year. Typical years of service and approximate failure risk allowable by the end-use customer were also identified.

The standard not only describes the characteristics of the nine use environments a recommendation is made for each condition as to how to determine the accelerated testing need to prove that the product will survive the expected end life conditions. The information from Table 1 is combined with some hypothetical example use conditions and used in some of the equations on solder fatigue a determination is made with some equivalent mean cyclic lives for the accelerated test conditions for both leadless and leaded surface mount solder attachments. These equivalent test cycles are determined for the range of Years of Service and the Acceptable Failure Risks in Table 1, but are the expected mean cycles to failure for the test conditions.

Table 1 End-use Environments Related to Solder Joint Wear-out and Fatigue

Worst-case use environment							
Use category	Tmin °C	Tmax °C	ΔT°C	t_D hrs	Cycles/ year	Typical years of service	Approx. accept. failure risk %
1) Consumer	0	+60	35	12	365	1-3	1
2) Computers	+15	+60	20	2	1 460	5	0.1
3) Telecom	-40	+85	35	12	365	7-20	0.01
4) Commercial aircraft	-55	+95	20	12	365	20	0,001
5) Industrial & automotive Passenger Compartment	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	10	0.1
6)Military Ground & ship	-55	+95	40 &60	12 12	100 265	10	0.1
7) Space leo geo	-55	+95	3 to 100	1 12	8 760 365	5-30	0.001
8)Military avionics a b c	-55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	10	0.01
9)Automotive under hood	-55	+125	60 &100 &140	1 1 2	1 000 300 40	5	0.1

The results show that for the more benign use conditions (Use Categories 1 through 6), the test regimes provide high acceleration factors; for the more severe use conditions, the test accelerations diminish or disappear entirely. This is the result of a number of reasons, such as severe thermal use conditions, long service lives, and low tolerances for failure acting singly or in concert. This reflects the fact that for these conditions the reliability of the products cannot be experimentally verified; reliability assurance has to depend solely on analytical reliability modeling.

Several additional technical papers have been published with the idea expressed that the strength of the solder joint and assembly was better than anticipated. No revisions have been made, or are contemplated as of this date by IPC, and the models that have been created by the IPC-SM-785 can still be used as a design guide for determining the methodology for testing the product to determine life cycle conditions.

When some of the industry was forced to move to new solder alloys that did not contain "Lead" the rules changed somewhat. New models were developed for the lead-free solders and some were very compatible with the existing work done by the SMT Accelerated Reliability Test Task Group, yet the new components being fostered on the industry require a new analysis. This is especially important with those components that are leadless and referred to as bottom termination components BTCs as shown in Figure 4. Some assemblers have forgotten that you needed solder volume under the part.

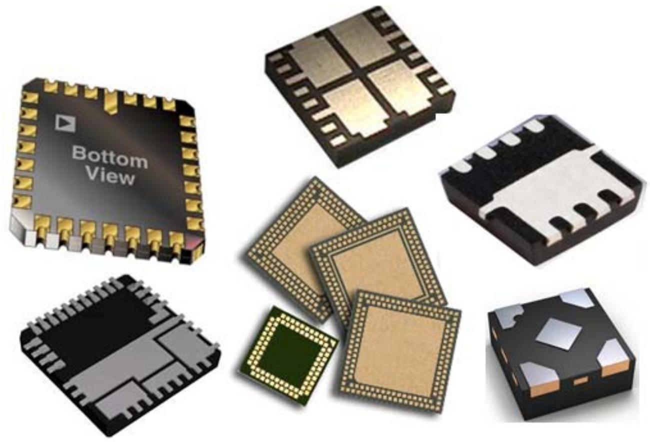


Figure 4 Bottom Termination Component examples

THE NEW RELIABILITY CHALLENGES

The world has changed to the point where most manufacturing is outsourced. Where at one time the electronic industry was made up of vertically integrated OEMs who designed, built, assembled and tested the product, the industry is now made up of a variety of partnerships with the biggest concern being that of Supply Chain Management. With that situation comes the fact that the designs have become much more complex. The traditional multilayer board has been replaced by HDI products that may consist of many steps in the manufacturing process to laminate a re-laminate the completed structure. Examples of descriptions abound such as 3-6-3 or 2-8-2 each describing a 12 circuit layer board however the manufacturing sequence and the occurrences of vias that run from layer to layer may be very different. See Figure 5 for various examples of HDI constructions.

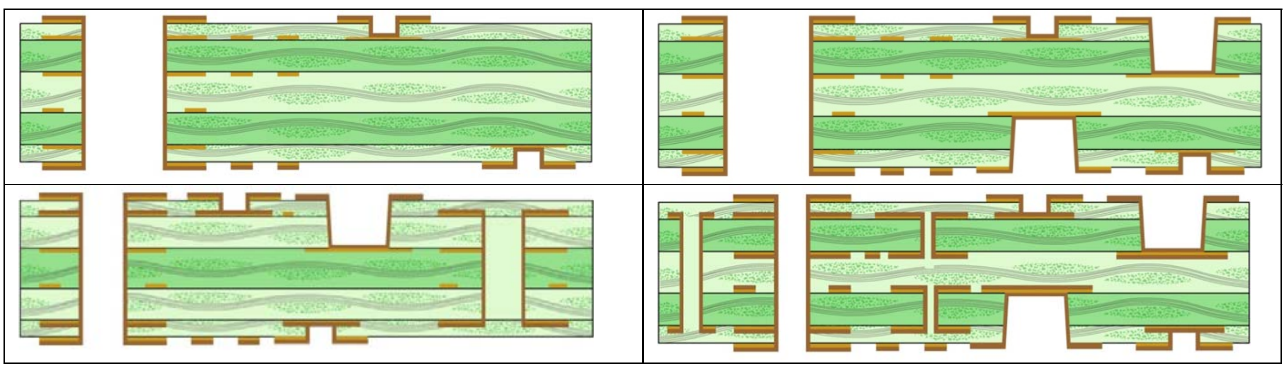


Figure 5 Examples of 4 different HDI products each requiring different process steps

With most of the complex printed board being outsourced the OEMs are struggling in order to determine the manner in which to convey the design concepts and the manufacturing requirements. In many instances the product will be described in the documentation package. This may consist of hard copy or electronic media. The manufacturing instructions are usually conveyed as Notes and in many instances reference industry specifications and the requirements that the customer wants delivered as part of his final product. These are the established requirements, but they do not guarantee the reliability of the product. The details establish the quality level required which is also predicated on the end-product use conditions.

Various performance classes have been developed by the industry and they are intended to convey the quality needed by the customer. The three classes established by the IPC are:

- ***Class 1 General Electronic Products*** Includes consumer products, some computer and computer peripherals, as well as general military hardware suitable for applications where cosmetic imperfections are not important and the major requirement is function of the completed printed board or printed board assembly.
- ***Class 2 Dedicated Service Electronic Products*** Includes communications equipment, sophisticated business machines, instruments and military equipment where high performance and extended life is required, and for which uninterrupted service is desired but is not critical. Certain cosmetic imperfections are allowed.
- ***Class 3 High Reliability Electronic Products*** Includes the equipment for commercial and military products where continued performance or performance on demand is critical. Equipment downtime cannot be tolerated, and must function when required such as for life support items, or critical weapons systems. Printed boards and printed board assemblies in this class are suitable for applications where high levels of assurance are required and service is essential.

The classes set the requirements for the quality of the final product; however they are not reliability descriptions. It is understood that without the quality the product can never achieve the reliability goals. Thus one should consider:

- **Quality** is the ability to produce the product in the manner specified by the customer in the documentation package provided, including any test or legal requirements. The concept is one of meeting the requirements. The OEMs define the printed board quality requirements necessary to meet their reliability needs.

- **Reliability** is the ability to function as expected under the expected operating conditions for an expected time period without exceeding expected failure levels. It is **Proof of Performance.** The End item reliability can only be determined by the OEM. PWB Fabricators often have little or no visibility to end item requirements.

The decisions being made for the arrangement of conductive layers in a Multilayer board are becoming more crucial every day. Not only is cost a player, but also availability of material in the thickness that various analyses would recommend. Add to these considerations the fact that traditionally board manufacturers have developed their own suite of preferred material; both thickness and suppliers. The issues are many on what a design requires electrically and what compromises can be tolerated in order to still get a **reliable working product**.

OEM products must survive 2 primary environments:
1) Product Assembly (Reflow/wave & rework)
2) Field Service (thermal cycles & shock/vibration)

Traditional PWB Quality Requirements are primarily measurements used for PWB fabrication process validation but have limited use for determining reliability. The modern reliability challenges are many. Components are much smaller than they were a few years ago. Components are placed more densely on the printed boards. The printed boards go through more severe reflow processes, and often multiple times. Lead-Free solder increases processing temperatures.

As a result printed board designs have changed where the board features are very small, with high aspect ratio vias (old designs seldom higher than 5:1, today can be 10:1) and there are many more vias per printed board than in the past. In addition laminate materials must be more robust as assembly temperatures are higher and the materials must have low z-axis expansion for greater via life.

Traditional printed board quality measurements are still necessary to collect the data necessary to keep processes in control. This is because features are smaller they are susceptible to process variation that might affect their reliability. It should be understood that checking 3 or even 12 holes per panel for quality does not provide a sufficient screen for defects. High volume thermal stress tests can sample many vias and pinpoint weaknesses that are used for process improvement.

Currently some common High Volume (large via count) Stress Tests are used by the industry as the measure of assessing reliability. These are identified as Interconnect Stress Test (IST) and Highly Accelerated Thermal Shock (Hats).

Interconnect Stress Test (IST) is an accelerated stress test method used to evaluate the integrity of the Printed Circuit Board (PCB) interconnect structure. IST creates a thermal cycle that stresses a specifically designed coupon, while simultaneously monitoring the electrical integrity of plated through holes (PTHs) and internal interconnects (Posts). It's a test method that measures the integrity of different areas of the same structure. IST tests the PTHs and the Posts at the same time.

Highly Accelerated Thermal Stress (HATS) was developed to emulate traditional air-to-air test methods, while significantly reducing the drawbacks of traditional methods. The test uses a single chamber in which high volume hot and cold air pass stationary samples. The high volume air flow provides rapid thermal transfer to the device under test and reduces the time for the specimens to reach temperature equilibrium. This greatly reduces the time required for each cycle, and the stationary samples are easily fixtured to a high-speed precision resistance sampling network

How do these tests relate to reliability is a tricky question that have caused a lot of soul searching by the OEMs. There is no easy answer. Some OEMs have been able to correlate IST or HATS test results to via life, others have not. Is an answer necessary? An answer is good to help establish OEM design rules but, If a PWB can be fabricated to survive, for example, 400 accelerated thermal cycles (IST or HATS) and proves reliable in OEM Product tests, then the 400 cycle limit can be used as a measure of process consistency that can assure PWB performance from lot to lot. It is a measure of the process capability as it relates to reliability failure modes and may not directly relate to final product reliability. It is a measure of the Printed board’s structure Durability.

End-Use Matrix for Printed Boards

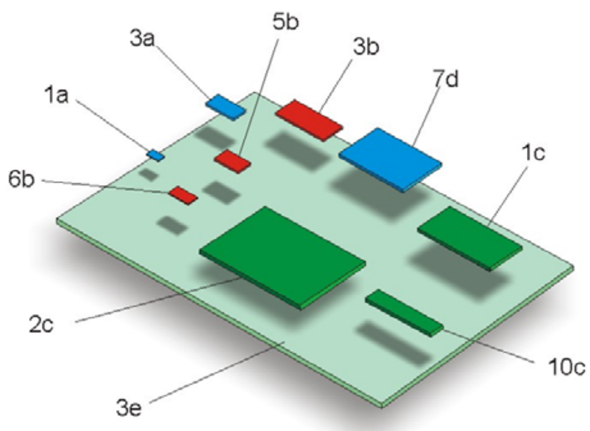
Building on the concept used to determine reliability for surface mount solder joints the end use environments are used to characterize the differences needed for checking reliability of different products. The printed board structures have been segmented into five categories of mounting products. These were:

- *Interposer:* from 5 to 50 mm L x W aspect ratio equals 1:1.5
- *Module:* from 10 to 75 mm L x W aspect ratio equals 1:3

- *Portable Board:* from 20 to 150 mm L x W aspect ratio equals 2:4
- *Product Board:* from 40 to 400 mm L x W aspect ratio equals 3:4
- *Backplan*e: from 100 to 800 mm L x W aspect ratio equals 3:6

The Interposer is used as a part of the semiconductor package. The Module is a small board that can be used many times and is mounted on a Product Board or Backplane. The Portable Board was established to accommodate those hand held products that needed finer features and greater precision. The Product Board is the mounting substrate used in most pieces of table top equipment, while the Backplane is the foundation of many systems that use the concept of daughter boards being inserted in the backplane unit.

The IPC Technology roadmap for the year 2011 used emulators to represent the products that provided an insight into the technology drivers for design, boards, assembly, and production sources. There were 14 emulators that represented the five mounting structures. Figure 6 show an example of the size variations of some of the products that were described in the roadmap which indicated their present characteristics and where they would be in ten years.



1a Consumer Interposer
3a Telecomm Interposer
3b Telecomm Module
5b Automotive Passenger Module
6b Military ground /shipboard Module
1c Consumer Portable Board
2c Computer Tablet Portable Board
10c Medical Portable Board
3d Telecomm Product Board
5d Industrial Product Board
7d Space Shuttle Product Board
9d Under Hood Product Board
3e Telecom Backplane
8e Military ATR Backplane

Figure 6 Emulator Board Size Comparisons

In order to establish some consistency between the end-use environments of the assemblies the same nine use conditions were identified as being representative of the industries uses of electronics. One slight change however became necessary since the industry has identified a specific need for electronics that are uses in medical equipment. As a result a tenth row was added to the matrix used to describe the reliability stress exposures that would be recommended for those products. The resulting matrix essentially consists of 50 cells that identify the needs of the 5 mounting platforms being used in the 10 end-use environments.

There is no doubt that just as in the 1970s the plated through hole was the weakest link, as the mounting structures have become more complex the stress simulation intended to establish the robustness of the interconnections needs to also match the environment. Cyclic stresses have always been used to establish the wear-out capability, so it is no surprise that they are used in today's methods of determining robustness. The differences between thermal extremes is important since it stresses the organic laminate material which when they expand add a stress to the interconnection barrel of the holes. Hole size and aspect ratio (hole length to hole diameter) also play a vital role in making the determination. The time that the stress is applied is a function of the use environment as are the extremes of temperature, humidity, or voltage surges that might be intended to simulate the field conditions.

Table 2 was developed to represent the testing of the mounting structure. It is only one example of what some OEMs feel is necessary in order to establish the robustness of the mounting structure. The OEM approach is to test the board material at 150°C, while the microvias, especially those that are stacked on one another, should be exposed to a cyclic condition of 190°C. The number of cycles is intended to establish the robustness of the product in each particular cell.

Table 2 Printed Board Construction to end-use Reliability Test Matrix

Product Application per end use					
End-use Environment	A-Interposer	B-Module	C-Portable	D-Product	E-Back Plane
1-Consumer	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150
2-Computers and Peripherals	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150
3-Telecomm	250 cycles @ 150	250 cycles @ 150	250 cycles @ 150	250 cycles @ 150	250 cycles @ 150
4-Commercial Aircraft	350 cycles @ 150	350 cycles @ 150	350 cycles @ 150	350 cycles @ 150	350 cycles @ 150
5-Industrial and Automotive Passenger Compartment	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150
6-Military (ground and shipboard)	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150
7-Space	1400 cycles @ 150	1400 cycles @ 150	1400 cycles @ 150	1400 cycles @ 150	1400 cycles @ 150
8-Military Aircraft	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150
9-Automotive (under hood)	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150
10- Bio Medical & Life support	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150

Since the advent of using lead-free solder in the assembly operation many OEMs now require some form of assessment that the mounting structure will pass the exposure. Most printed board assemblies are exposed to the reflow oven profiles needed during the attachment of components to one or both sides of the substrate. Since the components have a variety of different features in their profile as well as the mounting terminations these exposures may vary to several iterations. Add to this that after testing some components may need to be replaced. The OEM wants to be sure that after all the assembly work is completed that the mounting structures' integrity is still intact.

Table 3 is an example of the 50 cell matrix used to identify the number of cycles that a mounting structure might be exposed to during the assembly operations. They are usually worse case conditions and are intended to emulate the laminate characteristics that identify their Td (Temperature at Decomposition). The Td was a new requirement imposed on laminate descriptions that were intended to be used with lead-free assembly process profiles. The IPC-4101C defined several new formulations that were identified as being lead-free capable and therefore provided the Td as well as other pertinent electrical and physical properties.

These thoughts were considered when a group of reliability committee members were asked to develop the ranges identified in Table 3.

Table 3 Printed Board Assembly Simulation to end-use Reliability Test Matrix

Product Application per end use					
End-use Environment	A-Interposer	B-Module	C-Portable	D-Product	E-Back Plane
1-Consumer	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
2-Computers and Peripherals	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
3-Telecomm	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
4-Commercial Aircraft	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
5-Industrial and Automotive Passenger Compartment	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
6-Military (ground and shipboard)	6X230°C	6X230°C	6X230°C	6X230°C	6X230°C
7-Space	6X230°C	6X230°C	6X230°C	6X230°C	6X230°C
8-Military Aircraft	6X230°C	6X230°C	6X230°C	6X230°C	6X230°C
9-Automotive (under hood)	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
10- Bio Medical & Life support	6X230°C	6X230°C	6X230°C	6X230°C	6X230°C

CONCLUSIONS

The aspects of quality and reliability are the concern of every member of the supply chain. Deviations from the indented requirements, as documented by the OEM, are never a reason for acceptance as they filter back to the concept of dis-satisfied customers all along the supply chain; most of all the end-use customer. The industry and individual specifications identify the requirements for quality. These have been, and will continue to be, identified as:

- Visual Description
- Dimensional descriptions
- Interconnection Integrity (Microsection)
- Continuity/In-circuit test
- Customer Specific

With the need to establish a method of working with the members of the supply chain the OEMs need a new methodology to establish the fact that the new supplier, with slightly different materials and processes, can produce a product that is identical to that made during the prototype stages.

The term Process Robustness was coined by several OEMs to represent the test methods usually reserved for reliability evaluations now required of a new manufacturer. It is very similar to what the military once coined "First Article Inspection" and it may be for some contractual requirements that these issues will need to be revisited. The methods that would be used to establish "Durability" are:

- HATS test requirements
- IST test requirements
- Solder Float exposure
- Solder reflow simulation

These will become reliability requirements to ascertain product robustness.