PBGA SOLDER STRESS DEVELOPMENT MECHANISM ANALYSES UNDER RANDOM VIBRATION

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ABSTRACT
Large size commercially available plastic ball grid array chip packaging was tested and analyzed under random vibration to assess its application feasibility on satellite electronics. Two types of the PBGA were chosen, and the chips were surface mounted without underfill on a daisy chained polyimide printed circuit boards. Two strong levels of the random vibrations were applied sequentially to investigate the sustainability of the PBGA chips mounted on the polyimide PCB with aluminum frame. It was found that the test results did not show any solder failure under the test conditions, indicating the robust structural integrity and providing the evidences justifying the PBGA packaging application to the aerospace applications. Numerical analyses were also performed for the solder stress development mechanism. The results demonstrated that the first natural mode was not necessarily the dominant source for the maximum solder stress, and higher stress could be induced at higher natural modes depending on the chip size and its location.

Key words**:** PBGA reliability, Random vibration, COTS, Aerospace applications,

INTRODUCTION
The electronics packaging techniques employed for the satellite have been traditionally based on legacy, which usually lead to relatively heavy, bulky and expensive due to customized manufacturing. To overcome the pitfall, the applications of Commercially-Off-The-Shelves (COTS) such as PBGA chips have been suggested as a solution to the issues [1-3]. Recently, Kim and Hwang represented the PBGA packaging application analyses for the satellite electronics under very strong random vibration to simulate the launching situation [4]. They used 8 mm x 8 mm PBGA chips, a typical commercial application size, to manufacture test specimen coupons, and performed the random vibration tests monitoring the solder failures under two different test levels of acceptance and qualification. The applied power spectrum densities (PSD) of the levels were exceptionally high levels, which were known as one of the test conditions for the small and medium weights of low orbit satellite vibration reliability. This study is to investigate the PBGA packaging application to the satellite by using larger chips and PCB installation structure. A polyimide PCB was designed to a realistic size of actual electronics devices, and the large size PBGA chip was mounted to induce the solder joint stress. The entire specimen was tested under the two levels of power spectrum density, and the solder joint failures were monitored by in-situ resistance measurements to examine the sustainability of the chips under the vibrations. Generally, it is widely accepted that the maximum stress is generated by the first natural mode. To verify the presumption, numerical calculations were also performed for the detail solder stress development mechanism under the random vibrations by changing the chip sizes and their locations.
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SAMPLES AND EXPERIMENTS
Fig. 1 shows the test sample with PBGA chips mounted on the printed circuit board. Two different sizes of the PBGA of 16 mm x 16 mm (type-1) and 10 mm x 10 mm (type-2) with daisy chains were employed with Sn/Pb (63/37) eutectic solder full array, the number of which were 361 and 100, and the ball size 0.45 mm and 0.4 mm, respectively. No underfills were applied.

The power spectrum density of the random tests is shown in Fig. 2 (a). Two steps of the mean square acceleration levels per unit bandwidth of 0.35 g^2/Hz (acceptance level) and 0.7 g^2/Hz (qualification level) were employed, and the signal's root mean square values were 22.48 grms and 31.78 grms, respectively, in the frequency range of 20 ~ 2000Hz.

The sample was mounted on a pheumatic shaker following the power spectrum density levels. Two minutes of the acceptance level and three minutes of qualification level were applied for the tests. Fig 2 (b) reprensts the resistance measurements data at the qualification level. There was no failure found, which demonstrated the robust structural integrity of the PBGA chip packaging. To examine the PCB vibration behavior, an accelerometer was attached at near the chip P4, and the power spectrum density was applied again. Fig. 3 showes the measurement data, showing the multiple peaks were captured according to the sensor location.

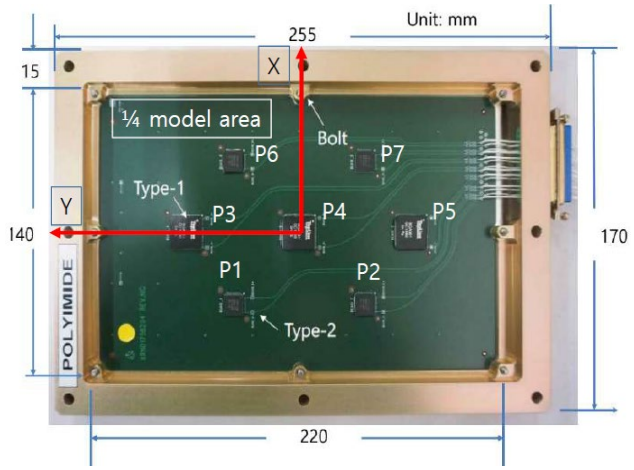
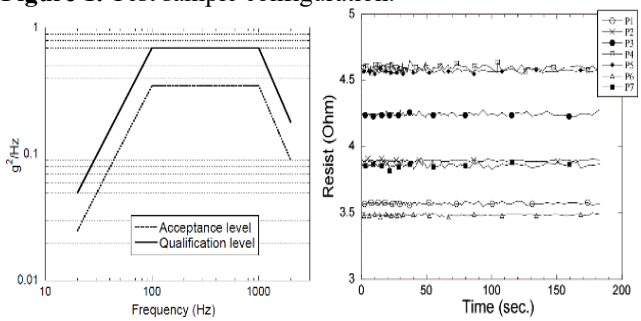


Figure 1. Test sample configuration.



(a) (b)

Figure 2. (a) Power spectrum densities of the two levels. (b) The solder resistance measurements during the qualification level.

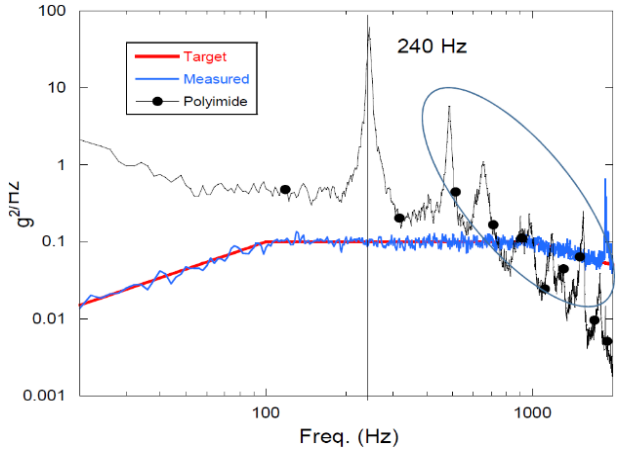


Figure 3. The PCB vibration behavior measurements under the random vibration.

NUMERICAL ANALYSES

Two types of the modeling for the sample, full model and a quarter model, were developed using ABAQUS 6.2. The natural frequencies and the corresponding modes were calculated by the full model using the PSD. Total 17 natural frequencies and modes were obtained between 20~2000 Hz, which would be the major sources of the solder stress developments.

For the solder stress calculations, to overcome the unacceptable computing time by excessive element numbers of the solders, the quarter model was used. The quarter finite element model is shown in Fig. 4. To cover the entire matural frequencies, the PCB boundaries were changed to four different boundary conditions (BC) of Xsymmetry-Ysymmetry (Xs-Ys), Xsymmetry-Yasymmetry (Xa-Ya), Xa-Ys and Xa-Ya. With the Xs-Ys BC, the first calculated mode is the first natural mode of the entire PCB. When the BC is Xs-Ya, the first calculated mode is the second natural mode of the entire PCB, etc.

Commonly, it has been widely assumed that the main source of the solder stress is the 1st natural mode, therefore the PCB center location is regarded as the most venerable due to the large deformation. The same assumption was taken in this study. As the first case, the calculation with Xs-Ys BC which implied the five natural modes including the 1st mode was performed. Then, the maximum stress was located in Fig. 5 (a), and found to be the corner of P4 chip solder (see Fig. 1). To cover entire natural modes, the BC was changed to Xa-Ys, Xs-Ya and Xa-Ya, and the accumulated stresses at that maximum node were collected and represented in Fig. 5 (b) as the RMS peel stress developments. As seen, the stress increased rapidly at around 225 Hz, indicating that the 1st natural mode was the dominant source of the stress development. The total maximum stress value was 102.5 MPa when all the values of each BC were added at the 2000 Hz.

The calculation results clearly indicated that the major stress was developed when the BC was Xs-Ys, where the first natural mode was affiliated. This results are in accordance with usual assumption that the maximum stress is occured at the edge of the center mounted chip due to the first natural mode.

As the second case, the quarter model was modified such that the P3 and P5 Type-1 chips were removed, and P6 chip was replaced by Type-1 chip. Same calculations as the first case were carried out by applying four boundary conditions. The maximum solder stress location was found at the corner of the center chip (P4) with Xs-Ys BC. Fig. 6 (a) illustrates the solder location, and the RMS stress profile at the maximum stress node is shown in Fig. 6 (b) with circle symbol. Again, the most stress was developed at about 240 Hz, the 1st natural frequency. The rest calculations of the three other BC's were performed, and their RMS stress profiles are shown in Fig. 6 (b) together. The next source of the stress was at about 670 Hz, the 5th natural frequency. The total stress was 102.5 MPa. Although there were slight contribution differences of the natural modes to the stress developments, the tendency of the stress development mechanism was very similar to the first case of Fig. 5.

Finally, the maximum stress under Xs-Ya condition was examined first in the same way as the second case. The location was found at the corner of the P6 chip as shown in Fig. 7 (a). Also, again, the three other calculations changing

the BC's were performed, and the stress development profiles at the node are represented in Fig. 7 (b). It is remarkable that the total RMS peel stress was 109.2 MPa, which is higher than the center chip (P4) maximum stress in the second case. Regarding the stress development contributions, unlike the second case, it was found that the second major source of the stress was the 4th mode, which induced the stress about 28 MPa, and the third source was the 3rd mode. The 1st mode was found to be the least source of the stress generation.

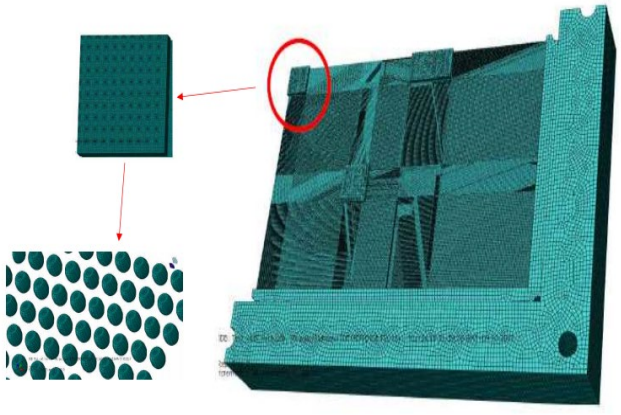
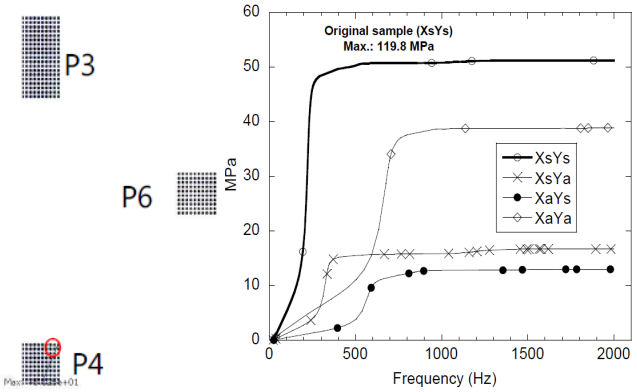
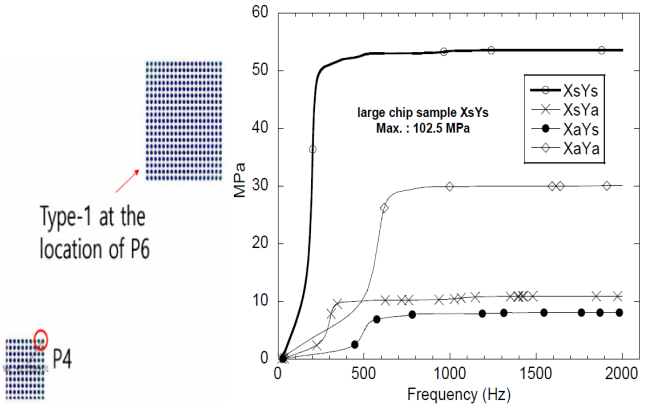


Figure 4. 1/4 model for the test sample.



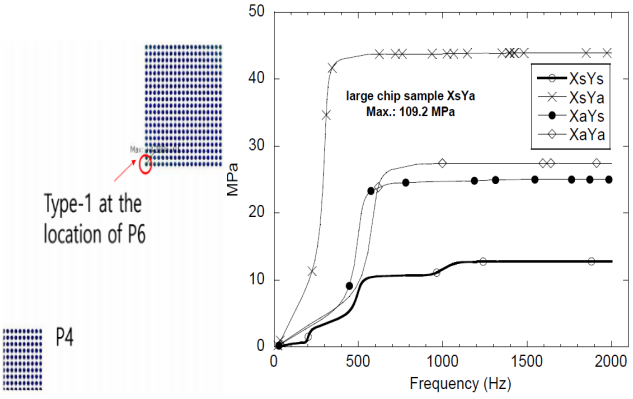
(a) (b)

Figure 5. (a) Maximum solder stress location at Xs-Ys of the sample using 1/4 model. (b)The stress developments by changing the boundary conditions.



(a) (b)

Figure 6. (a) Maximum solder stress location at Xs-Ys of the modified sample using 1/4 model. (b) The stress developments by changing the boundary conditions.



(a) (b)

Figure 7. (a) Maximum solder stress location at Xs-Ya of the modified sample using 1/4 model. (b) The stress developments by changing the boundary conditions.

The results indicated that, the effects of the natural modes are significantly dependent on the chip locations and size and the higher solder stress might occur at the chip located at the location away from the PCB center.

CONCLUSIONS

In this study, the strong structural integrity of the PBGA chip packaging was verified by testing the PCB with sizable chips under the harsh random vibration tests. The results showed a possibility of the COTS part applications to the satellite electronics devices.

In the given frequency ranges of the vibration, the natural modes were calculated by the numerical modeling. Also, the quarter model was developed and effectively used to examine the detail stress development mechanism by calculating different cases. The calculation results showed that the maximum solder stress of the test sample model was found at the corner edge of the center chip mainly due to the 1st natural mode, which was in accordance with the usual expectation. However, the modified modeling calculations by changing the chip size and location represented that the maximum stress was found at the chip located apart from the center. The unexpected results are from the stress development contributions of the higher natural modes than the 1st one, which have been frequently regarded as insignificant in the stress generation under vibration. In fact, in the modified sample calculation case, the 1st natural mode was found to be the least source of the maximum solder stress development. The results clearly demonstrated that, in the random vibration with the wide frequency range, the maximum solder stress location should be carefully investigated due to the fact that the dominant natural mode for the stress development is not necessarily the 1st one, and is dependent on the chip sizes and their locations.

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