As originally published in the IPC APEX EXPO Conference Proceedings.

Insulation Resistance of Dielectric Materials under Environmental Testing

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BIOGRAPHY

Stan Heltzel (1975) works at the Materials and Processes Division of the European Space Agency where, since 2008, he is responsible for qualification of printed circuit board manufacturers and technology. Analysis of PCB samples and exposure to simulated space environment occurs in the materials and components laboratories. From 2001 to 2008 Stan worked on environmental testing facilities in the lab, exposing materials and solar cells to simulated solar radiation. Stan has a Bachelor degree in Applied Physics.

ABSTRACT

For electrical equipment, current leakage in a printed circuit board (PCB) can result in intermittent or permanent failure. Current leakage can occur due to insulation resistance reduction between adjacent nets on a PCB. A working group of the European Cooperation for Space Standardization is drafting the standard ECSSQ-ST-70-12 on PCB design. Industry represented within this working group uses various design rules to define insulation distance as a function of voltage. The insulation distances are either based on material and design heritage or based on Generic Standard on Printed Board Design IPC-2221 [1]. The investigation involves measuring the leakage current within internal PCB layers in-situ during exposure of various specimens to a controlled ground-based test environment and a simulated space environment. This novel test method produced results which show breach of insulation resistance within fiber contaminated samples. This proposes a revision of standard IPC-4101 to implement tighter cleanliness requirements of laminate materials. Clean samples exhibit no breach of insulation resistance which confirms the rules proposed in the design standard.

1.0 INTRODUCTION

Insulation resistance testing has been used by the electronics industry as a tool for incoming inspection, material investigations and quality conformance. [2] The insulation resistance between two conductors is the ratio of the voltage to the total leakage current between the conductors. [3] Insulation resistance degradation can be caused by various phenomena. Electromigration is an electrochemical process that can occur when the conductive circuit of the PCB is submitted to an applied electric field in a humid environment, causing the electrodes to migrate in ionic form and redeposit elsewhere as a copper dendrite. Other electrochemical mechanisms include growth of a conductive filament from ionic contamination which typically occurs along glass fiber reinforcements within the laminate.

Conductive anodic filament (CAF) formation is a term used to describe an electrochemical reaction in which conductive paths are formed within a dielectric material due to transport of metal or metal salts through the dielectric. For CAF growth to occur, a bias and a path for this filament growth must be present, as well as a medium in which this electromigration can occur, i.e. absorbed moisture allowing dissolved ionic species to migrate and promote the electrochemical reaction that leads to CAF. [3] Insulation resistance measurements on PCBs are sensitive to environmental conditions. This behavior is primarily due to the fact that polymeric materials absorb moisture over time. This absorption can activate conductive contaminants on the substrate surface or in the base material of the substrate. [4]

Currently when considering the insulation distance within a PCB design, companies refer to material heritage and table 6-1 in standard IPC-2221A, specifically the rule 1 kV/mm for voltages above 70V. No test data was found to substantiate the guidelines of this standard. Insulation resistance is measured typically on the surface of a PCB, whereas the internal PCB layers have not been extensively investigated. Therefore a novel test method was developed to characterize insulation resistance in-situ as a function of environmental testing. The insulation resistance of the internal as well as the external layers in the PCB were included within this test method. This test method aims to demonstrate the reliability of the insulation distance as a function of voltage, which is in support of PCB Design Standard ECSS-Q-ST-70-12C.

2.0 EXPERIMENTAL PROCEDURE

2.1 Sample description

In this investigation a test voltage is applied across comb patterns. The leakage current is measured through the dielectric material which insulates the electrodes of the comb pattern. This leakage current provides information regarding the integrity of the material and its insulating properties.

PCB samples are designed with intralayer comb patterns, with internal and external layers as separate patterns, for insulation distances of 150 and 200 μm. A spacing of 100 μm is also used; however no patterns are included on the external layer PCB for this spacing as it is not consistent with typical manufacturing for space. The samples are arranged so that the 100 micron patterns have 6 internal layers with 2 patterns on each layer and no patterns on external layers. The samples that have 150 and 200 micron patterns have one pattern on both external layers, in addition to the internal patterns.

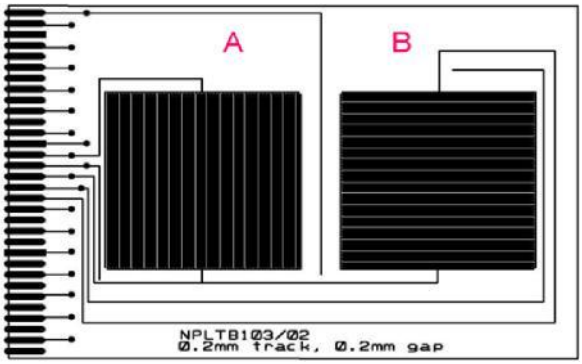

Figure 1: example of internal comb patterns

One PCB manufacturer 'A' produced samples using polyimide Arlon 35N and polyimide Arlon 85N materials. A second PCB manufacturer 'B' produced samples using polyimide Arlon 35N, to enable a direct comparison between the two manufacturers. In addition, manufacturer B also produced samples using high Tg FR4 epoxy Arlon 45N, to compare epoxy with polyimide. The samples are designed to slot into a connector which is attached onto the measurement apparatus. The thickness of the sample is 1.6 mm +/- 10% and the surface finish is galvanic nickel-gold on the connector pads and fused tin-lead on the comb pattern and tracks. Solder mask is used to facilitate the manufacture but is not part of the surface pattern of the test coupon. The samples do not have a conformal coating. Figure 1 shows an example of the comb patterns on an internal layer of the samples.

The number of squares within a comb pattern reflect the sensitivity of the sample. The number of squares is approximately constant; therefore the same sensitivity (gain) for each pattern is maintained. The number of squares within a PCB sample is calculated by dividing the track length by the distance between the tracks and multiplying that value by the number of repetitions of the pattern, as shown in table 1.

Table 1: Number of squares within test samples

Track width (mm)	Gap width (mm)	Pattern height (mm)	Pattern length (mm)	Squares Per Row	Number of rows	Total squares
0.10	0.10	20.6	20	200	103	20600
0.20	0.20	40.4	40	200	101	20200
0.15	0.15	30.3	30	200	101	20200

2.2 Test Equipment

This investigation uses the Gen 3 Systems AutoSIR® Insulation Resistance Testing System to evaluate the insulation resistance by measuring leakage currents in the picoamp range. Figure 2 shows the experimental setup. The AutoSIR allows accurate resistance measurements to be made up to 10^{14} Ω. The test rack used for this investigation can hold up to 16 test coupons and can monitor up to 256 channels at intervals from minutes to days. Each channel is current limited (by using a resistor of 1 MΩ) which should ensure that any dendrites are preserved for failure analysis and to protect the measurement equipment.

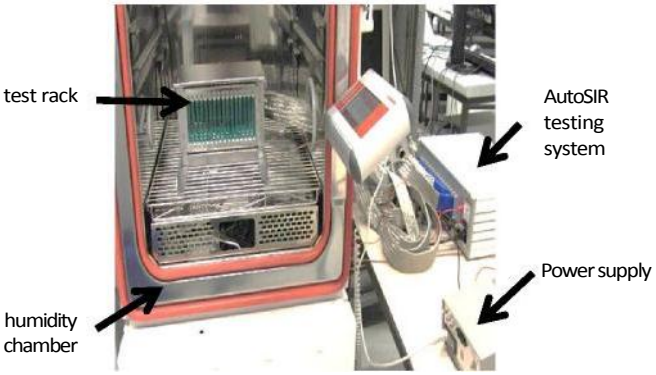

Figure 2: Experimental setup

The equipment enables continuous monitoring of leakage current between comb patterns in-situ. The wires are PTFE insulated and the data acquisition card design minimizes channel-to-channel leakage. This is important as extremely low level currents involved in SIR measurement cause stray electromagnetic noise or leakage between wire insulations to affect accuracy. [5] Within the experimental setup the PCB samples are slotted into the test rack attached to AutoSIR test system, as shown in figure 3. The test rack is placed inside a humidity chamber. An external power supply can be attached to the system for voltage above 100 VDC or for AC voltages.

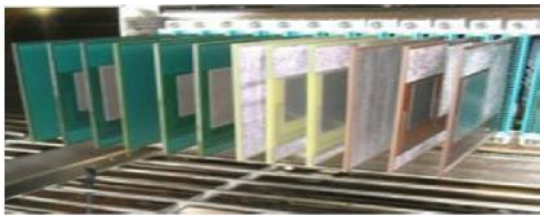

Figure 3: Samples slotted into test rack

2.3 Test Procedure

The test procedure used for this investigation is shown in figure 4. The samples are benchmarked at an ambient environment of 50% relative humidity (RH) at 25oC, before being submitted to an ageing environment of 75% RH at 85oC for a prolonged time period to determine if electrochemical migration (ECM) occurs. This is the temperature, humidity, bias (THB) part of the test program, during which leakage current measurements are conducted. Prior to thermal cycling, this first THB part is named Phase 1 and highlighted in blue within figure 4.

Thermal cycling is then conducted according to the standard ECSS-Q-ST-70-10C [6], with the samples submitted to 200 thermal cycles (T/C) from -65°C to +135°C to evaluate the effects of space environment. No leakage current measurements are performed during the thermal cycling part of the test program. Before and after thermal cycling, the samples are submitted to a bake out of 120°C for 6h to avoid unwanted damage due to the high humidity within the board and to remove thermal history prior to ambient THB testing. After thermal cycling, the resistance was reassessed in the chamber through THB testing phase 2 highlighted in green within the test plan.

The samples are then submitted to 300 more thermal cycles from -65°C to +135°C and reassessed again by THB testing. This is described as Phase 3, which is highlighted in purple within the test plan. Finally, there is a repetition of the ambient benchmark test, which is described as Phase 4 and highlighted in red.

It is important for this experiment to apply the bias continuously. It is practical to apply just a single voltage during the test. Regarding the AutoSIR equipment, it is not possible to use multiple voltages simultaneously in conjunction with external power supplies. The AutoSIR can accommodate a maximum voltage of 500V from an external power supply.

1)	Bake out	6h@120°C	
2)	THB ambient	24h, 50%RH, 25°C	Phase 1:
3)	THB ECM	150h, 75%RH, 85°C	THB at 100 VDC before T/C
4)	Bake out	6h@120°C	
5)	T/C 200x	-65°C to +135°C	
6)	Bake out	6h@120°C	
7)	THB ambient	24h, 50%RH, 25°C	Phase 2:
8)	THB ECM	150h, 75%RH, 85°C	THB at 100 VDC after 200x T/C
9)	Bake out	6h@120°C	
10)	T/C 300x	-65°C to +135°C	
11)	Bake out	6h@120°C	
12)	THB ambient	24h, 50%RH, 25°C	Phase 3:
13)	THB ECM	150h, 75%RH, 85°C	THB at 100 VDC after 200+300x T/C
14)	Bake out	6h@120°C	
15)	THB ambient	24h, 50%RH, 25°C	Phase 4: final ambient THB at 100 VDC
16)	Microsectioning		

Figure 4: Test Procedure.

This paper reports on results obtained with a bias voltage of 100 VDC. On the pattern with the smallest insulation distance of 100 µm, this results in an electrical field of 1kV/mm, as proposed in chapter 1. Note that the test method was designed using the IPC-TM-650 method 2.6.14.1 as a guideline [7] and the test setup used IPC9201A as a guideline [2]. The intention of this procedure is to stress the PCB with margin to accelerate failure, if there is any. The selection of environmental parameters is based on several pre-tests and on the heritage with environmental conditions for space simulation.

2.4 Microsectioning

Microsectioning is vital for a detailed assessment of board quality as a good microsection reveals how efficient the manufacturers are regarding important processes for board reliability. [8]

After the electrical test phases, the samples are investigated in order to locate and analyze the cause of any defects and failures. This failure detection involves looking at the samples under an infrared camera whilst supplying a current to any specific internal pattern that remains in a failed condition at the end of the THB test program (during phase 4). The current heats up the sample locally which can be detected by the infrared camera for localization of the hotspot on the sample with a marker. The current is kept as small as possible to prevent overheating the small defects and subsequent damage. Then, the samples are microsectioned at the relevant internal layer in order to visualize the cause of the failure. SEM-EDX analysis is also conducted to investigate any possible copper migration paths or for contaminant analysis.

3.0 ELECTRICAL TEST RESULTS

Figure 5 illustrates how the different test phases are represented within the result graphs, showing the logarithm of insulation resistance of all patterns within the sample over time. Each phase starts with the ambient THB test, which benchmarks the insulation resistance. This is followed by the ECM THB test during which a drop in resistance can be observed over time due to the increased humidity and temperature. In between each phase thermal cycling takes place. This occurs without insulation resistance measurements and is, therefore, not represented in the graph.

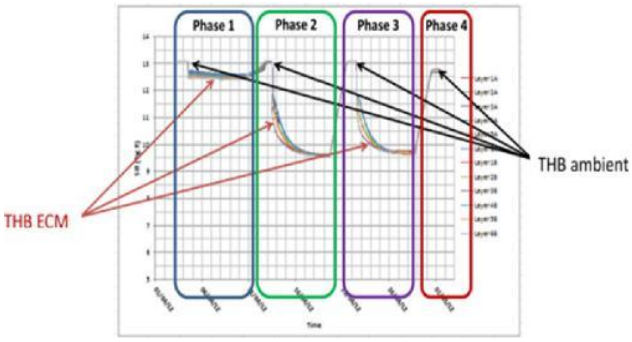

Figure 5: Typical result graph showing the logarithm of the resistances of all patterns during the 4 test phases.

In phase 1 the resistance drop is small, but after thermal cycling in phases 2 and 3 the resistance drop becomes more significant. The decrease of insulation resistance at the end of the phase with respect to the initial benchmarking during ambient THB in phase 1 is named "delta" resistance (in table 2). At the start of each phase it can be seen that the resistance recovers during the ambient THB part, almost to the initial value as measured in phase 1.

Figure 6 shows a typical graph of samples of manufacturer B made of epoxy Arlon 45N for one spacing only. The other two spacing's are not included in this paper as they behave almost identical. The inset in figure 6 shows a magnification of the resistance drop during phase 2. During the start of the ECM THB test in phase 2, it can be seen that the layers close to the sample surface react faster than the layers underneath, which react again faster than the layers in the middle of the sample. The correlation between the time constants of the resistance drop and the position of the pattern within the Sample demonstrates that the resistance drop is caused by the diffusion of humidity through the sample.

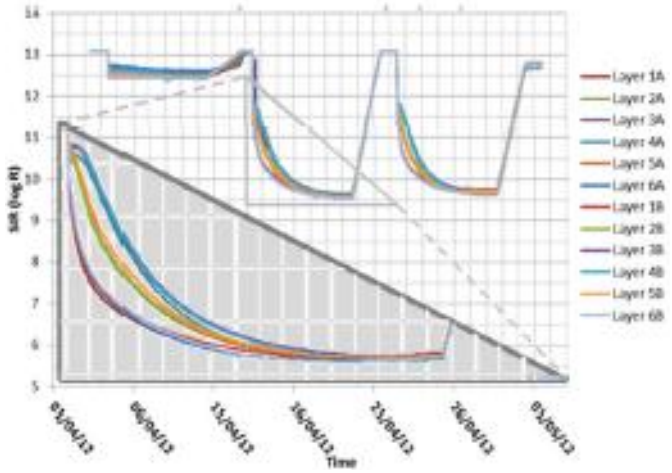

Figure 6: 100µm Arlon 45N by manufacturer B

Figures 7 to 9 show the logarithm of the insulation resistance over time for the internal patterns of the Arlon 35N samples by manufacturer A. Figures 10 to 12 show the equivalent graphs for the Arlon 35N samples by manufacturer B. In addition to the general changes in insulation resistance as explained for figure 5, it can be seen that some traces behave noisy, with sudden changes in resistance of many orders of magnitude. These are considered failures in insulation resistance.

Table 2 summarizes the results of all graphs obtained during the test program. The resistance values within the table are all written in scientific notation, i.e. 13.1 is equal to $10^{13.1}$ Ω. The table displays an overview of the THB test phases with the samples grouped by material and manufacturer. The average resistance at initial ambient condition is shown in the table, as well as the resistance magnitude change within the "delta" column. The failed patterns at each phase in the testing process are also shown within the table. The definition of a failed insulation resistance is the sudden reduction of insulation resistance by orders of magnitude, which can be repetitive or continuous and shows a behavior that is different from non-failing coupons and characteristic for electromigration. [9]

The samples of manufacturer A made of Arlon 85N behave in a similar manner as the samples of Arlon 35N for that manufacturer, except that more failures are observed as reported in table 2. Therefore these graphs are not included in this paper.

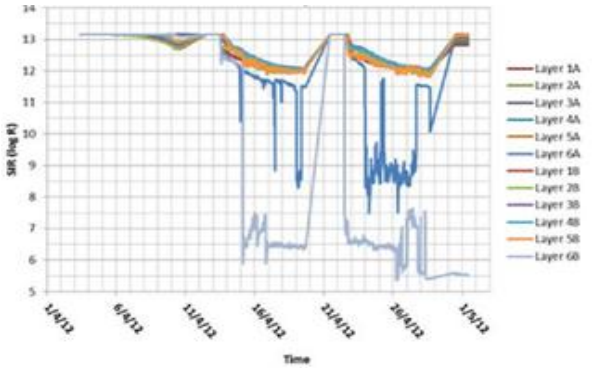

Figure 7: 100µm pattern Arlon 35N by manufacturer A

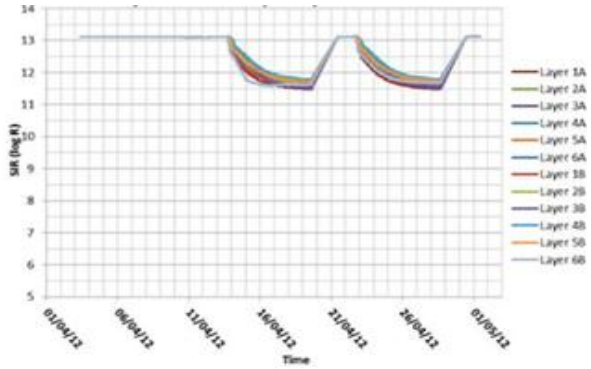

Figure 8: 150µm pattern Arlon 35N by manufacturer A

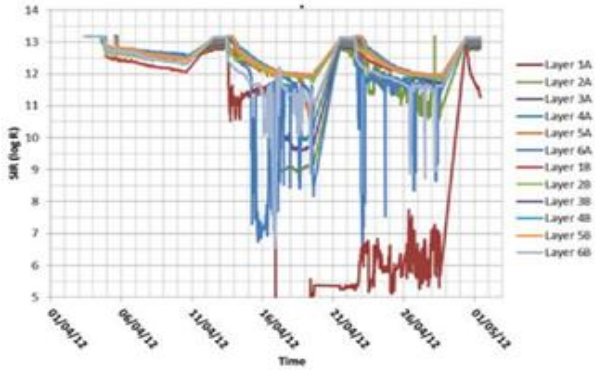

Figure 9: 200µm pattern Arlon 35N by manufacturer A

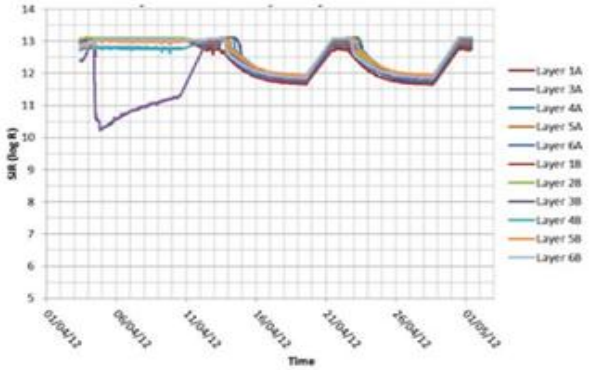

Figure 10: 100µm pattern Arlon 35N by manufacturer B

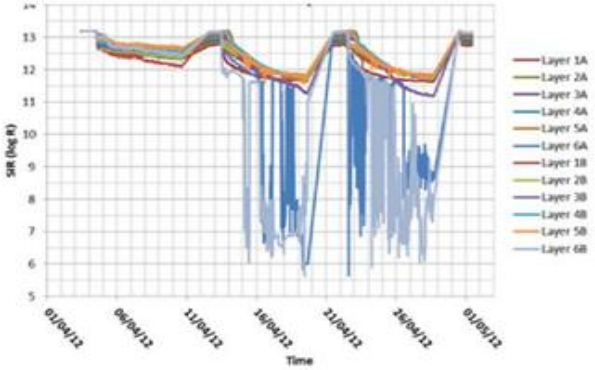

Figure 11: 150µm pattern Arlon 35N by manufacturer B

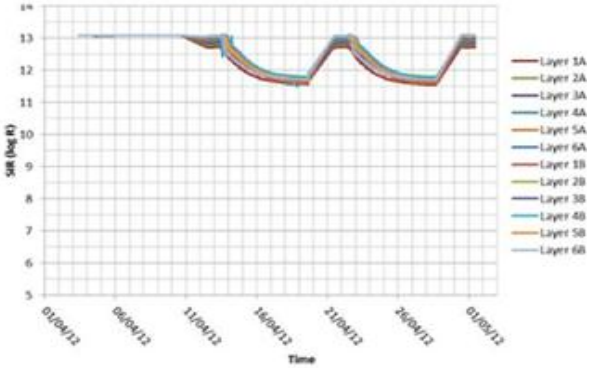

Figure 12: 200µm pattern Arlon 35N by manufacturer B

Table 2: Electrical results summary

Board	Phase 1 - THB before TC			Phase 2 - THB after 200TC		Phase 3 - THB after 200TC + 300TC		Phase 4 - Final Ambient THB	
	initial R THB ambient [log Ω]	delta R THB ECM [log Ω]	number of failed patterns	delta R THB ECM [log Ω]	number of failed patterns	delta R THB ECM [log Ω]	number of failed patterns	delta R THB ECM [log Ω]	number of failed patterns
Man. A - 85N	13.1	0.7	0	1.1	12	1.0	14	0.3	6
Man. A - 35N	13.2	0.6	0	1.6	8	1.5	7	0.1	1
Man. B – FR4 45N	13.1	0.5	0	3.4	0	3.3	1	0.4	0
Man. B – 35N	13.0	0.2	0	1.2	0	1.2	0	0.0	0

4.0 ANALYSIS OF ELECTRICAL TEST DATA

Manufacturer A – polyimide Arlon 35N
(figures 7, 8 and 9)

There is a high insulation resistance of about 1013 Ω at the beginning of phase 1, which decreases less than an order of magnitude during the ECM THB test. There are no patterns failing. In phase 2 after 200 thermal cycles the resistance recovers at the ambient THB test. Then it decreases more significantly during the ECM THB test and 8 patterns are failing. This repeats in phase 3, with 7 patterns failing. During phase 4 the average resistance mostly recovers and so do most of the patterns that failed intermittently. However, 1 pattern does not recover and remains in a failed condition.

Manufacturer A – polyimide Arlon 85N

(graphs not included in this paper, see table 2)
These samples behave similar to polyimide Arlon 35N of the same manufacturer A, except that more patterns are failing. During phase 1, again no patterns are failing. Twelve patterns fail during phase 2 and 14 patterns fail during phase 3. During phase 4 some patterns recover but 6 patterns remain in a failed condition.
Manufacturer B – polyimide Arlon 35N (figures 10, 11 and 12)

The general trend of these samples is similar to the trends observed on the polyimide samples of manufacturer A. However, no significant failures of insulation resistance can be observed during any of the phases. Only pattern 3A (purple trace in figure 11) shows lower insulation resistance during phase 1, but this trend is not characteristic for electromigration. This is not considered to be a failure. During phases 2 and 3, again the typical decrease of resistance can be observed as was seen for all other samples. This is not considered to be a failure.

Manufacturer B – FR4 epoxy Arlon 45N
(figure 6)

The general trend of insulation resistance is again similar to the polyimide sample of both manufacturers, with only little resistance reduction in phase 1 and a more significant decrease in resistance during phases 2 and 3. It can be seen that layers close to the surface are affected faster by the reduced resistance than internal layers because of diffusion characteristics of humidity. The decrease in insulation resistance in phase 2 and 3 is three orders of magnitude for the epoxy samples, which is larger compared to about 1 order of magnitude for polyimide. This indicates that the material is affected more significantly by the thermal cycling.

There is only one pattern (on 200 tm pattern, not shown in fig 6) that fails repeatedly during phase 3, which recovers in phase 4. All other patterns do not show failure of insulation resistance.

The general decrease in insulation resistance in phase 2 is of the same order as in phase 3 for all samples. This indicates that the material is significantly affected during the first 200 thermal cycles and no further changes occur during the subsequent 300 cycles. It is not within the scope of this paper to investigate the cause for the general decrease in resistance, but less intimate adhesion after thermal cycling between resin and glass reinforcement could be a possible degradation mechanism. The initial value of insulation resistance is the same for all insulation distances used. This is because the pattern size is adapted to keep the number of squares the same, as explained in table 1. The amount of failures and the time until failure cannot be correlated to insulation distance. This unexpected observation will be explained in the next chapter.

5.0 MICROSECTIONING RESULTS

Table 2 shows that some of the patterns fail intermittently in phases 2 and 3 and recover in phase 4. The patterns that remain in failed condition at the end of the test program are suitable for further testing by infrared thermography and microsectioning in an attempt to localize and visualize the defect.

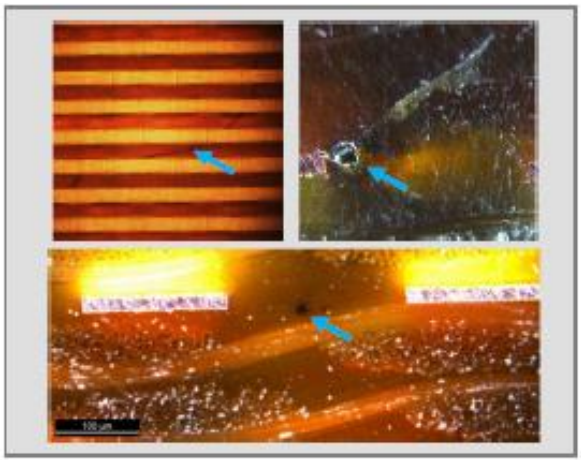

Figure 13: Fiber contamination in prepreg
left: top view above the plane of the fiber
right: cross section of fiber near conductor and crack propagation in dielectric material after electrical overstress
bottom: cross section of fiber in the prepreg between 2 conductors

Figures 13 and 14 illustrate the defects found within the samples. No defects are found that can be attributed to degradation of the dielectric material or PCB construction (delamination, micro-cracking, etc.). All defects found are associated with fiber contamination of the prepreg. SEM analysis of short-circuit defects shows copper migration across dielectric material. It was identified that the fiber contamination is probably nonmetallic but further analysis is needed to achieve more details on the elementary constituents of the fibers.

The first step in the ECM mechanism is path formation. The fiber contamination can provide a path for the next steps of ECM, which are electro-dissolution, ion transport, and electro-deposition. [11] If this step is delayed, the overall dendrite formation rate required for ECM failure is decreased. Many types of contaminants and impurities could be present on the samples. These contaminants can originate from various sources such as material-based impurities, insulator components and residues from the plating process or the board. Dust, wear particles and volatile pollutants could also cause contamination within the samples. [10] If the contamination within the sample contacts two metal surfaces at different electrical potentials, irreversible copper anode corrosion and migration of the conductive corrosion products can occur. This happens until a short-circuit appears within the sample. [5] This is shown in figure 14.

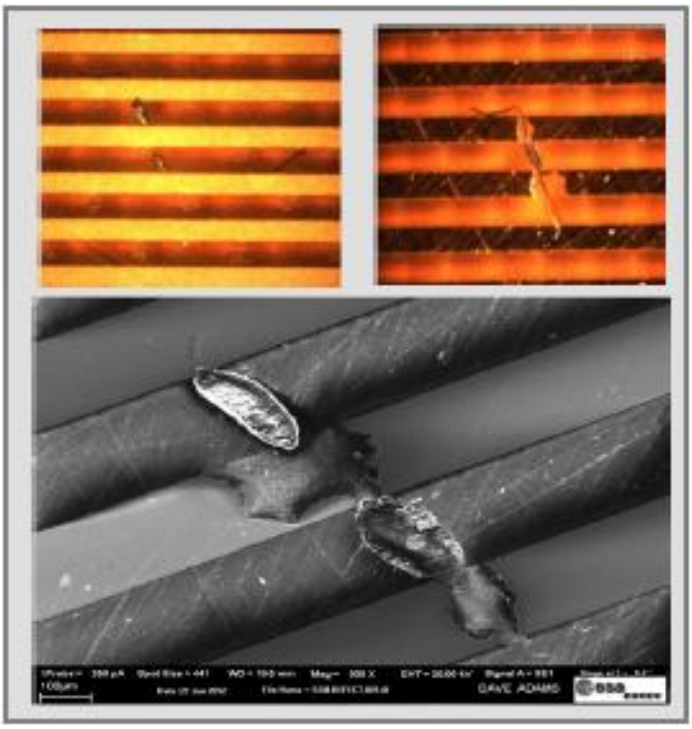

Figure 14: Copper migration along fiber contamination
left: top view above the plane of the fiber
right: top view in-plane with the showing consumed copper at the conductors and redeposit ion of copper along the fiber
bottom: SEM image of copper migration along fiber

The large size of the fiber contamination with respect to the 100, 150 and 200 jtm insulation distances with which the comb patterns are designed, explains why the extent of failure of insulation cannot be correlated with the insulation distance, as was noted in chapter 4. Particulate contamination is a known problem on prepreg and on copper clad laminate. Note that base materials are typically procured against specification IPC-4101C [12]. Clause 3.8.3.1.6.f. of that specification allows fiber contamination up to 13 mm length. This investigation shows that such large fibers are unacceptable for high-reliability applications in worst-case environmental conditions with small spacings and high electrical field.

6.0 CONCLUSIONS

The following conclusions can be drawn based on the general trend of insulation resistance change:

1. The general insulation resistance during THB decreases significantly after thermal cycling. Second set of thermal cycles does not further affect the resistance drop.
2. The insulation resistance of epoxy boards decreases more than for the polyimide boards.
3. Continuous resistance decrease after thermal cycling is not considered a failure of insulation resistance as it does not indicate electromigration.

The following conclusions can be drawn based on the observations of failed individual patterns:

4. No internal or external patterns fail in the THB testing before thermal cycling.
5. About 20 patterns fail on samples of manufacturer A, whereas no significant failures are observed for manufacturer B. The samples made from Arlon 35N are made by both manufacturers and are directly comparable.
6. For all samples where the defect was found by microsectioning, breach of insulation resistance is associated with fiber contamination, not with dielectric breakdown.

The following general conclusions can be drawn:

7. The design rule of 1 kV per mm insulation distance between internal circuit tracks does not cause dielectric breakdown after thermal cycling with margin, provided that no contamination is present.
8. The requirements for PCB base materials as detailed in IPC-4101C may not be adequate to prevent breach of insulation if worst-case imperfections are indeed present in the PCB. This is a particular concern for space industry because of the high-reliability applications and worst-case environment.

7.0 FURTHER WORK

Further investigation at 200 VDC has been performed. Analysis is on-going at the time of submitting this paper. Nevertheless, preliminary observations confirm the findings made in this paper.

AC bias voltage could also be used in future experimental setups to investigate different mechanisms of dielectric breakdown. Samples made with a wider variety of materials could be tested with the same test procedure, or a new procedure could be developed in order to test the insulation resistance of a via to a plane or interlayer between planes.

8.0 ACKNOWLEDGEMENTS

This work was performed as a Young Graduate Trainee project at ESTEC, and could not have been completed without the help of the TEC-QTM section within ESTEC, as well as the PCB manufacturing companies.

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