IN-LINE TESTING OF HIGHLY PANELIZED PCBAS WITH PARALLEL FUNCTIONAL TEST

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ABSTRACT
As semiconductor manufactures continue deliver more capabilities in ever smaller packages, most circuit board assemblies are shrinking. High volume electronic modules are increasingly manufactured in panels of 10, 20, or even 40 identical boards. The increase in panel density is driving substantial efficiency and throughput gains on the SMT lines; however, the typical testing processes is unable to match this increased throughput.

Traditional test process throughput can easily be 5-10x slower than production throughput for these boards. This mismatch in throughput capability is forcing manufacturers to choose between high levels of untested work in process (WIP) inventory or giving up the throughput gains by slowing down the SMT line.

New technology is available to provide simultaneous electrical functional testing of all the boards in the panel, allowing test to occur in line with production. System architecture, application development, and integration will be discussed. Process benefits, including case studies, will be provided, as will industry trends that drive manufacturers to reduce human handling and scrap reworked boards. Lastly, the status of these technologies, current capabilities, limitations, and commercial rollout plans detailed.
Keywords: Functional test, Panelized PCBAs, Industry 4.0, Test throughput

INTRODUCTION
Today, we'll discuss the manufacturing process challenges faced by electronics manufactures producing large panels of small boards.

Spring semester of my freshman year in college, I was studying for a Physics final and asked a Senior friend and Electrical Engineering major how he memorized all these formulas. He answered, 'F=ma, you can't push on a rope, and derive the rest." Needless to say, this was not especially helpful advice.

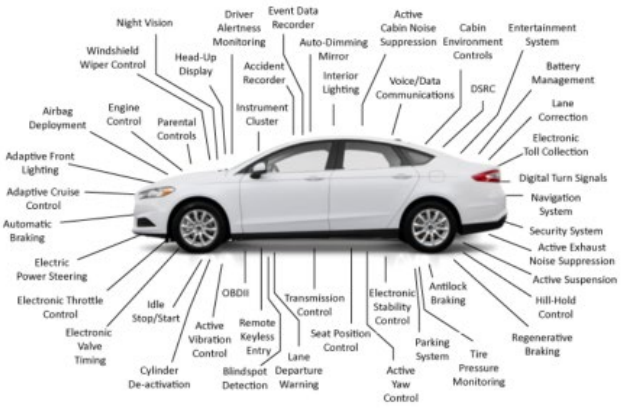
Let's start where everything starts in modern electronics: Moore's Law. The relentless doubling of the density of transistors that drives the major trends of our industry. Simply put: Chips get smaller, faster, and cheaper. Repeat. Of course, this is not a surprise, it's the foundation of the electronics industry.

Within this context, there are two types of circuit boards: boards that push the limits of current chip technology and boards that perform limited functionality. Examples of 'Max' boards are the current telecom network router boards, a densely packed next generation cell phone, or advanced Mil/Aero application. While we have many boards pushing the limits, the vast majority of circuit boards produced today have limited capabilities that do not require the same level of complexity.

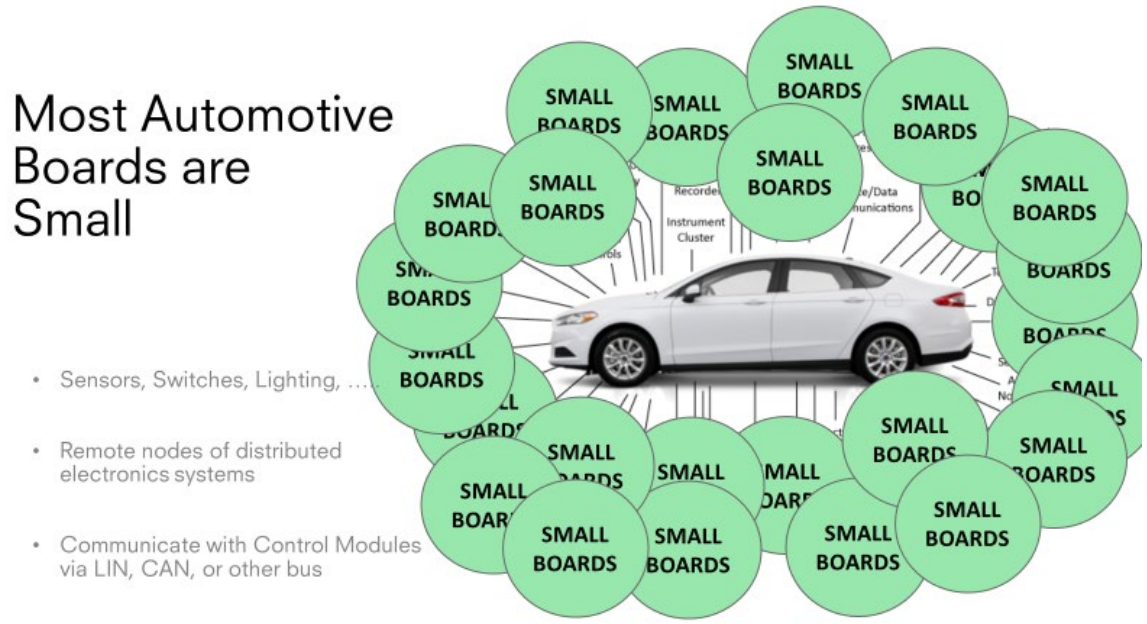
In the automotive electronics industry, we see examples of both types of boards. The architecture of electronics systems in today's cars puts the computing power in a few 'controller' units: the engine control unit, the navigation and entertainment system, and, in some cars, the electronic powertrain controller. These max boards are greatly outnumbered, however, by smaller, simpler assemblies that provide remote capabilities and communicate back to the control unit.

Electronics Throughout

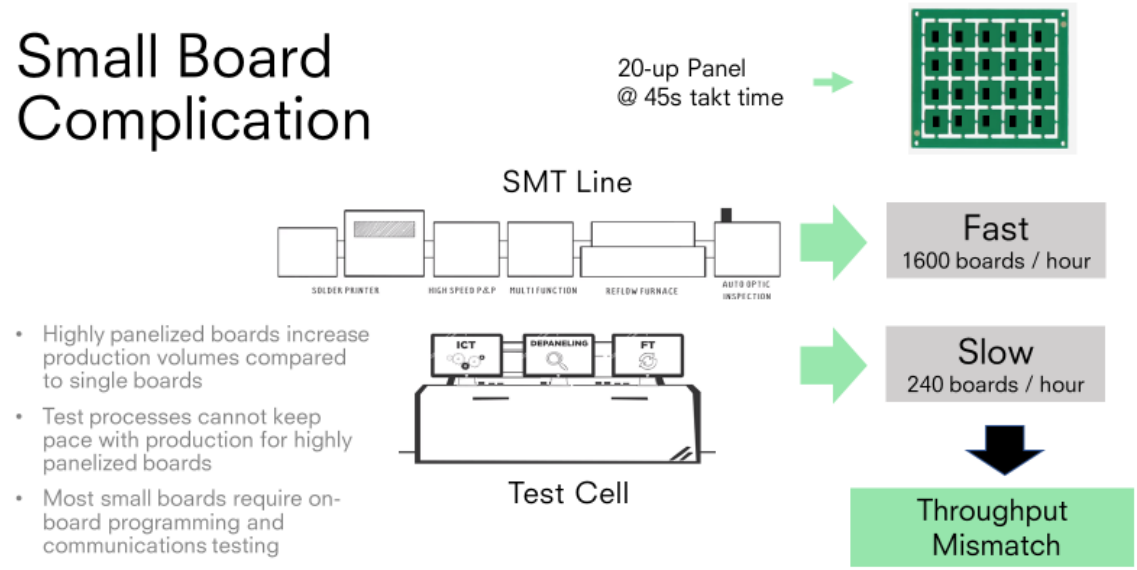
- Sensors, Switches, Lighting, ...
- Remote nodes of distributed electronics systems
- Communicate with Control Modules via LIN, CAN, or other bus



Each of these small boards has a job whether it is to activate a remote sensor, flip a switch, or turn on a light, the board is controlled centrally and reports back either on the CAN or LIN bus (with a few exceptions). These jobs are important, but they rarely stretch the capabilities of modern electronics. The capabilities of these boards are defined by one or two key chips depending on the precise functionality. Due to the automotive industry's volumes, these chips are nearly always custom designs specific to a model or platform. Small boards are manufactured in panels to optimize the efficiency of SMT equipment. In automotive, panels of 10, 20, or 40 boards are common. A recent project was a 400-up panel of tiny consumer product boards which is extreme today, but panel density will continue to trend upward.

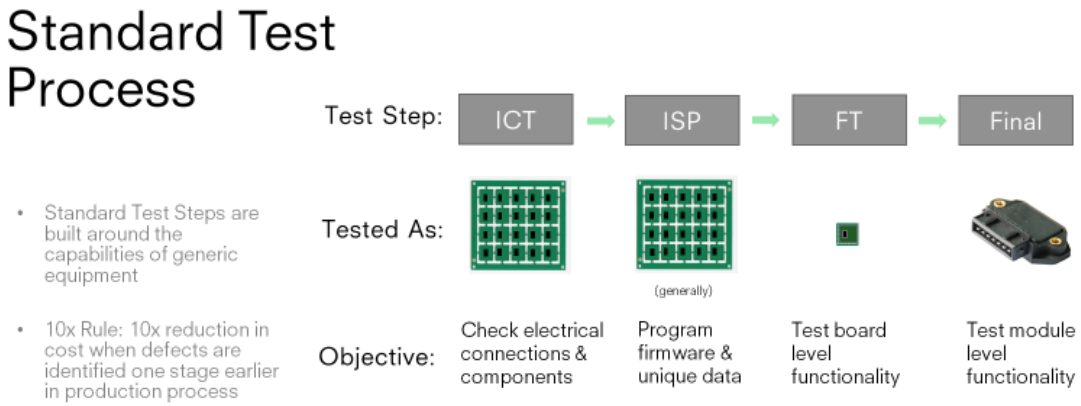


SMT equipment produces panels of small boards just as fast as a single board, so the takt time or beat rate of the line is similar. Consequently, the velocity of boards leaving the SMT line is proportionally higher than traditional larger boards. For example, a 20-up panel produced with a takt time of 45 seconds generates 1600 boards per hour, whereas a 1-up panel would only produce 80 boards. Sometimes, we forget the simple math that a 20-up panel means 20x more boards flying off the line. This increased velocity of production is the cause of the problems we see for manufacturers of small boards. Plainly, the test process is not capable of keeping up with the SMT line's supersized production.



As an example, let's look back at that 20-up panel to explain what happens. First, you'll notice that we're not on the SMT line anymore. Typically, manufacturers deal with the highly variable test times experienced across a range of boards by taking it offline – to the test cell. There, four processes are typically seen: In-Circuit Test,

On-Board Programming of the chips, De-paneling, and electrical functional test. It's worth noting that there is generally another functional test step, but that does not occur until the board has been assembled into the complete module. Each manufacturer determines the test specification and where each functional test occurs. Some tests can only occur once the module has been assembled and other tests, especially for sensor boards, are not electrical in nature.



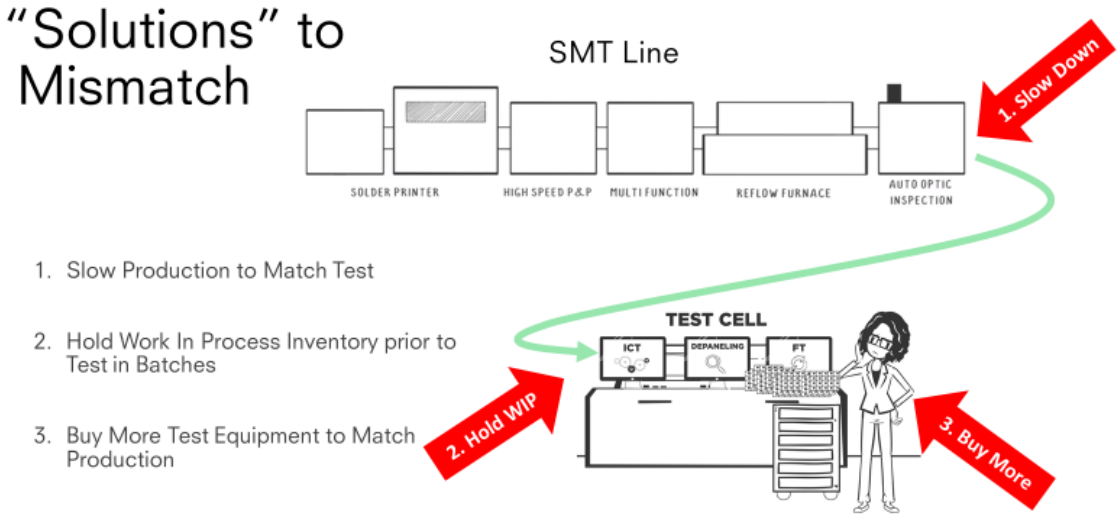
In-Circuit Test is conducted on the panel as the first step in the test cell. Generally, on-board programming accompanies ICT on the same system. De-paneling follows, then Electrical Functional Testing of the singulated board. Because each panel has turned into 20 boards, the functional test time of 5 seconds is accompanied by 10 seconds of handling. So, a single panel of boards takes 5 minutes to run through the electrical functional test station – those 300 seconds represent nearly 7x longer than it took to produce the panel, primarily due to the increased handling time as one panel becomes 20 separate boards. This 'Throughput Mismatch' is the key driver of challenges for manufacturers of highly panelized boards.

Interestingly, the Mismatch is not really caused by slower test than normal, it's caused by faster production. Highly panelized boards have a much higher velocity of production than other boards and traditional test processes cannot keep up.

Manufacturers have found three paths to addressing the Throughput Mismatch. First, they can slow production to match test throughput. While uncommon, we have seen this at a major automotive factory where lines are slowed to 1/3rd of capacity to avoid the other two problematic "solutions" discussed below.

Second, production can shift to a batch mode where a specific product is produced for several hours, building up Work-in-Process (WIP) Inventory which is slowly processed by the test cell. Depending on the volume requirements of the product, the magnitude of the mismatch, and the batch size, manufacturers can build WIP inventories of 1,000 to 10,000 boards several times per day. Because of the high velocity of production seen when manufacturing highly panelized bords, even typical automotive volumes do not require continuous production from the line. In general, one shift is usually sufficient to produce a highly panelized product at typical automotive electronics volumes of 2-3 million parts per year for a product.

Third, manufacturers can staff and equip the test cell so that it matches the throughput of the SMT Line. This solution is expensive and is generally only seen in extremely high-volume production where the SMT line must produce continuously.



Each of these 'solutions' has costs and trade-offs. First, slowing down the SMT line avoids the WIP Inventory issue, but is expensive and reduces production flexibility.

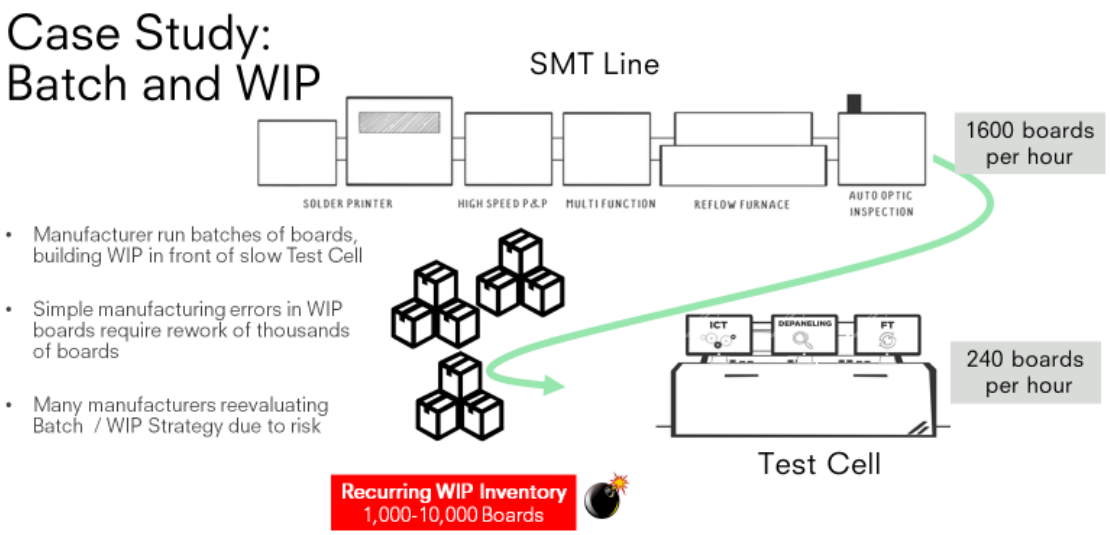
Batch process is probably the most common method we see in the automotive electronics industry. This strategy is immediately visible when you visit a factory, as the WIP inventory is hard to miss. Unfortunately, most 'Batch' producers also have a story about the time they produced 5000 boards with the same simple manufacturing defect. Depending on their customer's rework policy, this can be an expensive or extremely expensive side effect. Given that the WIP Inventory is built up multiple times per day, it is only a question of when the defects will happen. In addition, the WIP inventory is difficult to manage and takes up considerable space on a busy production floor.

Newer lead-free processes can be much more difficult to test after a few hours of oxidation. The surface of the test pads develops a crust as it oxidizes and is more difficult to penetrate for the bed-of-nails probes. These contact issues are a nuisance and lead to false failures that take time to detect and address.

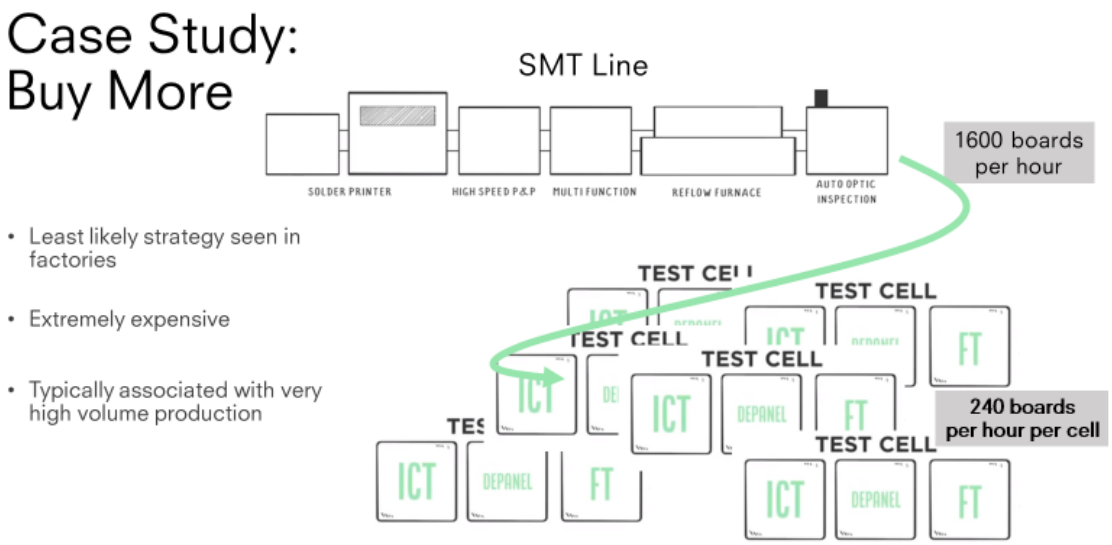
More importantly, the 'Batch' process is becoming untenable given automotive OEMs reluctance to allow rework of any kind. At present, most safety products are not allowed to have specific types of rework if at all due to the uncertain nature of that process.

Another complication for the 'Batch' process is the lack of real-time test data. Industry 4.0 and all the benefits thereof require the collection, communication, and analysis of data in real-time. Test equipment is a key source of data for the system, but, that data is significantly less valuable and actionable if it is four hours old because the boards sat in WIP inventory until the test cell could catch up.

As stated above, despite these process and quality trade-offs, 'Batch' process is the most common solution for addressing the Throughput Mismatch of highly panelized small boards.



Lastly, manufacturers can match the throughput of the SMT line by purchasing enough Test Equipment to keep up. This approach is only seen when production volumes are extremely high such that the SMT line needs to operate continuously. In these cases, the high-volume production justifies the additional cost for the manufacturers. However, these extreme volume cases are rare and most manufacturers accept the process challenges associated with the Batch Process.



The Big Problem Testing Small Boards is a process challenge. Each manufacturer has weighed the trade-offs and chosen a testing process that is viable. Yet, given the trend codified in Moore's Law, we know that the challenge will only increase as panel density increases.

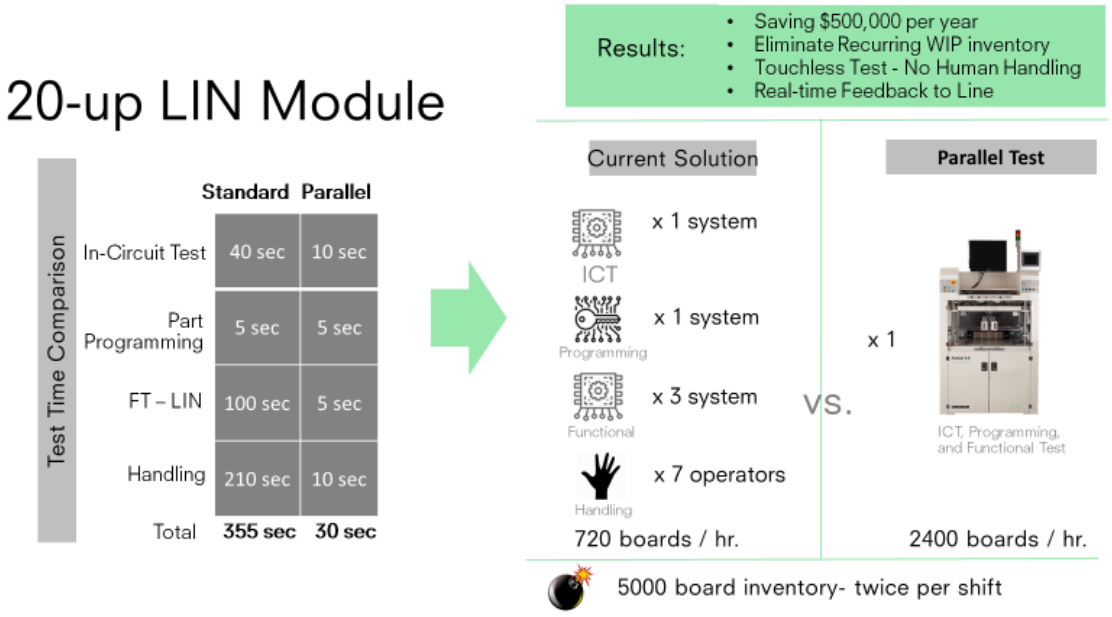
Against this backdrop, a new technology has been developed to address these process challenges. The technology has a simple yet powerful promise to assist manufacturers by enabling the Parallel Functional Testing of an entire panel simultaneously.

Using our previous example, Parallel Functional Testing of all 20 boards reduces the functional test time from 100 seconds to 5 seconds and eliminates 200 seconds of handling time. Because ICT and Programming times are generally fast for these products, it is often possible to have one system conduct ICT, On-Board Programming, and Functional Test on a single test system that can match the takt time of the SMT line, so, inline testing is possible. In addition, an Inline Test System sufficiently fast to keep up with the SMT line enables the production and distribution of real-time test data, a precursor to implementing Industry4.0.

Why is parallel testing so much faster than the traditional, manual functional test? Parallelism provides the same effect for each test step, so the longer the test step, the greater the benefit derived from testing in parallel. For example, 20-resistor measurements that take 25 milliseconds each will take half a second if done individually and only 25 milliseconds if done in parallel. It's 20 times as long, but it's still a relatively short time improvement. The lengthiest test steps for small boards are communications tests. Since most small boards are communicating back to a controller via a serial bus, the communication back and forth must be tested. With all the delays and back and forth, this process can take several seconds for each board.

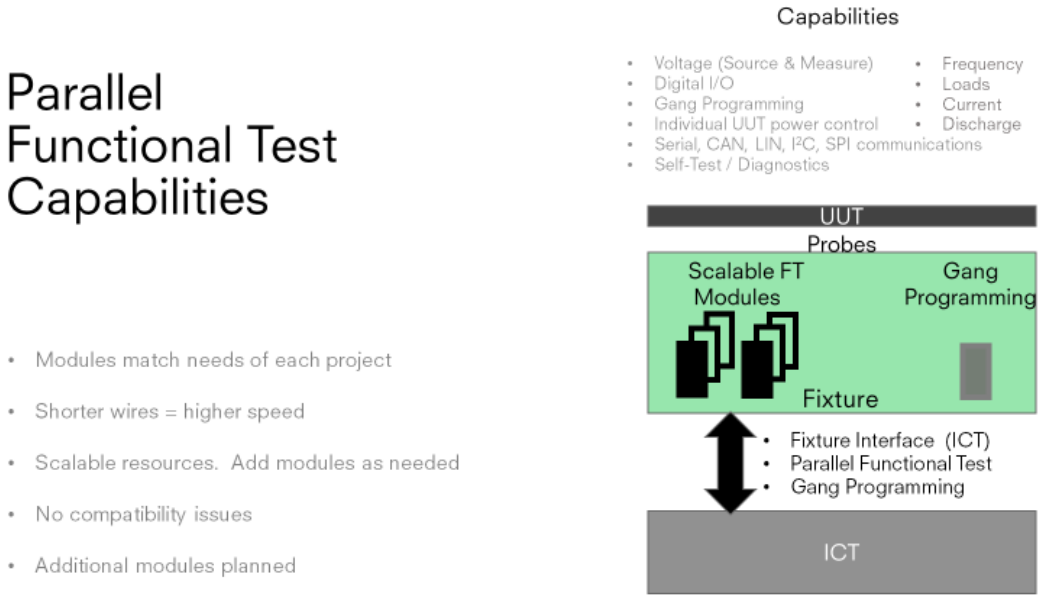
Longer still is the manual handling time for each small board post de-paneling. The industry generally assumes that it takes 10 seconds for an operator to put a board on a test fixture and take it off after testing is complete. A 20-up panel then generates 200 seconds of manual handling. Importantly, manual handling is not something the industry wants. It is expensive, is the source of defects, and adds complexity and variability to the test process.

Parallel Functional Testing eliminates the problem of handling small boards and enables inline testing. Touchless test has been a goal of the industry for many years. Parallel Functional Testing is making it a reality for highly panelized boards.



Of course, it has long been possible to develop functional testers capable of testing more than one board at a time. However, the new Parallel Functional Test Technology is available combined with an In-Circuit test platform and On-Board Programming capability, allowing an In-line, all-in-one approach that greatly reduces complexity of the test process.

Electrical Functional Test must meet a wide range of test requirements, so any functional test platform must have a corresponding set of capabilities. In the instance of highly panelized boards, an additional challenge of providing sufficient channels of each required test capability exists and threatens to make the solution impractical in typical test platforms.

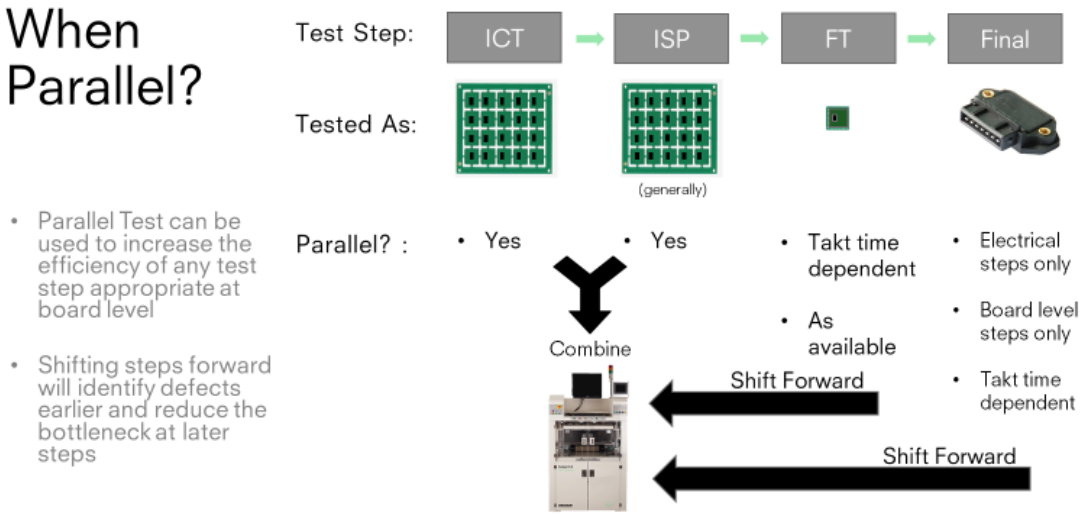


The new approach provides a range of individual test modules each capable of providing at least 8 channels of a given functional test capability. These modules are daisy chained and connected by a proprietary communications bus that allows control by the In-Circuit Test platform. The configuration of modules needed for each functional project is unique and is assembled inside the test fixture to minimize wire length, yet, provide for performance of the specified functional test steps.

As with any new technology, manufacturers need to find the most valuable use that fit their specific products, operations, and business strategies. Key to identifying optimal use cases is the fact that Parallel Functional Test is not a change in test specification, merely a method to conduct a specified set of tests earlier and more efficiently for a specific class of electronic assemblies.

As manufacturers examine the potential benefits of parallel testing, several process benefits emerge: Enabling Automation, Reduced Human Handling through Touchless Test, Increased Throughput, Earlier Test Results, and Reduction of Test Cell Activities. Manufacturers must weigh the potential benefits for their product mix and specific test requirements.

Not all tests are feasible for parallel testing. For example, many final functional test steps require that the module be assembled. A pressure sensor assembly may have an embedded electrical self-test that is appropriate for parallel test, yet, still require an actual physical pressure test at module level. Other test requirements may not be appropriate or available to be conducted in parallel, such as radio frequency communications.



Inline test requires analysis and planning of takt time optimization. In most factories, test operations are conducted off the SMT line in the test cell. The offline approach frees test strategies from the strict limit of the SMT line takt time, yet, the byproducts of this approach are additional handling, WIP Inventory, and delayed test results. Shifting test steps to the line demands additional planning to optimize process benefits while respecting takt time.

Yet, respecting takt time restrictions is a simple requirement for production equipment and an issue manufacturing engineers well understand. As our industry shifts to intelligent digital systems, we recognize that the Test Cell is a compromise that limits our ability to fully realize new opportunities. Offline processes are inherently manual. WIP Inventory is inherently risky and 4-hour old information is not compatible with Industry 4.0 principles.

Parallelism in test works for small boards built in dense panels, but, parallelism doesn't help for boards that aren't panelized. Parallel test does not cut the 5 minute In-Circuit Test time for that leading-edge networking board or the 15 minutes needed to run the on-board self-test. But we should not forget that we are still operating

on the steep slope of Moore's Law and the vast majority of boards will continue to shrink in size even as they get faster and cheaper.

In summary, small boards create numerous problems for electronics manufacturers because of the mismatch between production throughput and test throughput. This mismatch has been addressed by manufacturers in three ways: slowing production, batch processing with WIP Inventory buildup, and adding test capacity to match production throughput. Each of these approaches has costs and side-effects for manufacturers.

A new kind of test technology utilizes simultaneous functional testing of the entire panel of small boards. Parallel Test provides benefits to manufacturers by matching SMT line throughput. The major benefits of this new technology are: Enabling Inline Test to eliminate human handling, Provide Real-Time Data to Intelligent Digital Systems, Eliminate the need for WIP Inventory, reducing rework issues, increasing throughput and efficiency, and simplifying the process by eliminating test cell operations.