GLASS PANEL PACKAGING, AS THE MOST LEADING-EDGE PACKAGING: TECHNOLOGIES AND APPLICATIONS

Rao Tummala, Bartlet Deprospo, Shreya Dwarakanath,
Siddharth Ravichandran, Pratik Nimbalkar,Nithin Nedumthakady, and Madhavan Swaminathan
3D Systems Packaging Research Center, Georgia Institute of Technology
GA, USA
rao.tummala@ece.gatech.edu

ABSTRACT

The semiconductor and systems landscape are changing dramatically. As Moore's law begins to come to an end for many reasons that include minimal increase in transistor performance and in computer performance from node to node but at higher power, the industry has begun to shift to interconnections, referred to as Moore's law for Packaging. This focus addresses both the need for homogeneous and heterogeneous integrations by interconnecting smaller chips and smaller components with higher performance at lower cost and interconnecting them as multichip in 2.5 and 3D architectures. This is also called extending Moore's law, not in a single chip but with multiple chips interconnected horizontally and vertically. This strategy is very consistent with the dramatic and emerging changes in electronic systems such as in HPC, AI and a new era of self-driving and electric cars that potentially think and drive better than humans. This requires device, packaging, and computing architecture paradigms with an entirely different vision and strategy than transistor scaling alone. Packaging, which can be viewed broadly as system scaling, is now viewed as replacing Moore's law for enabling better devices and better systems, unlike in the past.

Glass packaging is being developed by Georgia Tech and its industry partners, as the most leading-edge packaging, consistent with the above systems needs in cost, performance, functionality, reliability, and miniaturization. This paper describes the critical glass packaging technologies, their R&D and commercialization status as well as all the current and future applications. It compares and contrasts glass packaging against other leading-edge technologies such as Si and embedded packaging.

Key words: Insert here to aid in searches.

INTRODUCTION

Since every device must be packaged ,for the device to be tested and assembled onto the board, packaging, defined as primarily interconnecting, has evolved from dual-in-line (Dip) with 16 I/Os to ceramics, organic laminates, embedded and silicon packaging, as shown in fig. 1.This plot is very similar to the Moore's Law plot, except the number of transistors are replaced with the number of I/Os. In this figure, silicon packaging is the most leading- edge packaging with as many as 200, 000 I/Os currently. So, what will replace Si packaging is the focus of this paper. While Si packaging has many advantages such as the manufacturing infrastructure for ultra-high I/O density, but it also has many shortcomings too. The purpose of glass packaging is to address these shortcomings. These shortcomings include high electrical loss and high dielectric constant at material level, high RC delays at interconnect level, perfectly matched TCE at device level but totally mismatched at board level, and high cost of manufacturing of large packages beyond 15 mm in size.

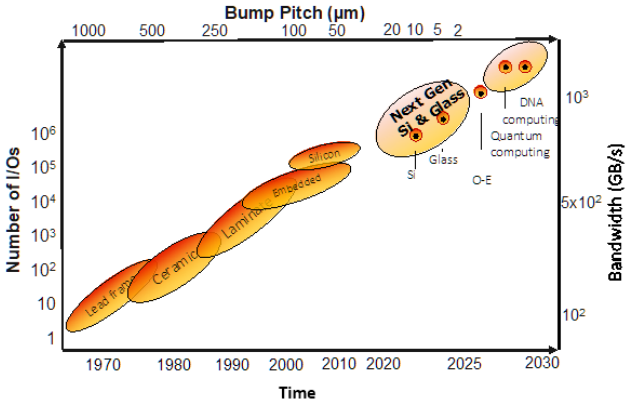

Figure 1. Moore's Law for Packaging I/Os; exponential evolution of I/Os in the last six decades

ARCHITECTURES AND APPLICATIONS

Advanced packaging architectures for heterogeneous and homogeneous integration can be classified as 2.5D and 3D, based on how ICs are integrated. In 2.5D approach [1], ICs are interconnected in a side-by-side fashion on an interposer such as Si interposer, while in 3D approach, chips are vertically stacked, typically, by means of Through-Silicon-Vias (TSV).The 3D stacking of memory on top of logic or vice versa has been thought of as the best packaging approach to achieve ultra-high bandwidth. While such an approach enables the shortest interconnect length, it is fundamentally limited by two issues: (1) real estate required for extremely large numbers of TSVs in the logic IC for power and signals, and (2) high thermal dissipation from the logic IC that is in the stack. This led to two developments: (1) Apply 3D with TSVs only for memory stack, with much lower number of I/Os, and (2) develop 2.5D to remove heat from the exposed logic ICs. Such an approach provides a short-term solution to achieve homogeneous and heterogeneous integrations prior to 3D.

Packaging architectures can also be classified as chip-last and chip-first. In chip-last packaging, the substrate is first fabricated, and the ICs are then assembled on the top; whereas in chip-first, the ICs are embedded and then substrate wiring is then deposited as the first step of processing. Both these approaches have their advantages and disadvantages. Chip-first packages enable ultra-thin form factors, avoid the need for chip-level assembly, and propose a way to scale I/O count without assembly limits. However, such an approach poses the thermal challenge as the backside of the die is not exposed for conventional thermal management. Embedding expensive dies also poses a challenge for bare- die fine-pitch testing. While chip-last solves the thermal and known-good-die (KGD) problems, these packages are still limited in I/O pitch due to assembly scaling and throughput. Although newer technologies such as hybrid bonding offer potential for < 10 µm I/O pitch, the processes continue to be challenged by the need for ultra-clean, smooth and highly planar oxide surfaces [2].

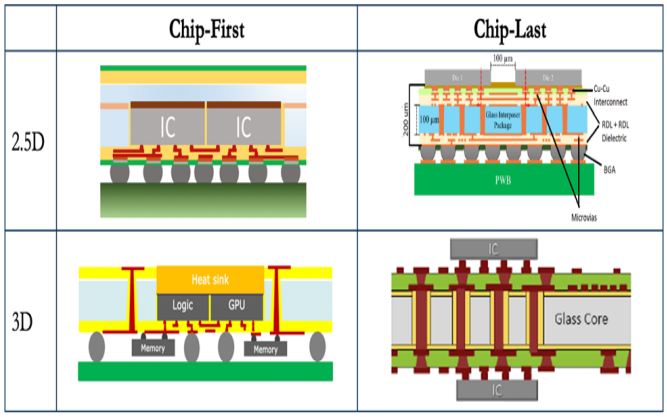

Figure 2. Glass Packaging Architectures developed at Georgia Tech

GLASS SUBSTRATE, TPV AND RDL TECHNOLOGIES

Georgia Tech has been developing glass as a packaging substrate technology in both chip-first and chip-last and in both 2.5D and 3D architectures for a wide variety of applications like high-speed digital, RF, 5G and mm-wave, mems and sensors and high power. Georgia Tech began the next generation of 2.5D interposers using glass panels in both chip-last and chip-first versions to address three limitations of conventional silicon interposers: (1) lower cost even for larger packages, (2) direct attachment t of the package to PWB, and (3) better electrical performance with lower RC delays, with a focus on lower line resistance using high aspect ratio conductor traces [3]. Georgia Tech has demonstrated, with its industry partners, TPV formation processes around 10,000 vias per second at fine pitch in 100 micron-thick glass substrates. Georgia Tech has targeted 2.5D interposers to be produced from large 510 x 510 mm2 panels so as to reduce the overall cost per interposer. Any interposer that is as large, as 50 mm or larger in size, must be assembled with reliability to both ICs and board, requiring CTE for the core to be around 7 ppm/K. The CTE of silicon is about 3 ppm/K. Glasses can be synthesized and are available in CTEs ranging from 3 to 9 ppm/K. Glass with CTE of 7 ppm/K can be a large BGA package for direct assembly to the board, unlike with silicon. In addition, Georgia Tech has developed advanced materials and lithographic processes to demonstrate very small lines down to 1 µm and also developed high aspect ratio conductors with 4X reduction in line resistance at 1 GHz. Figure 2. Glass Packaging Architectures developed at Georgia Tech are shown in Fig. 2 showing chip-first, glass panel embedding (GPE) 3D architecture for power-efficient-high-bandwidth computing. Since the memory dies are assembled at fine pitch on embedded glass substrates, the interconnects between the Logic/GPU and the memory is shortened, multi-fold [4]. Such an architecture does not need TSVs in the logic die to achieve such short interconnect lengths. The proposed architecture also has the potential to address the thermal issues, that are created in 3D IC stacks, through novel package-integrated thermal management architectures.

Glass is one of the oldest- known materials. It has evolved recently, however, to serve a variety of applications that include automotive, computing, communications and very large displays. Glass in electronics is not new. The total usage of glass in area is more than that of silicon. Both emerge, however from sand. Glass is manufactured in 100's of compositions to serve these and other applications. Unlike IC- grade- silicon, which can only be grown as small round cylinders, up to 300 mm in size and then cut, ground and polished, glass can be drawn from molten state in ultra-thin thicknesses and to ultra-fine surface finishes. Many through via technologies in glass have been explored and developed in the last 10 years. These include mechanical drilling, wet etching, laser drilling, gas-discharge drilling as well as a combination of wet and laser drilling technologies.
Redistribution layers are the most value-add technologies in all of packaging, as they provide the highest I/Os. To form these in multilayers, dielectrics are used as insulators between the copper wiring layers to achieve isolation and drive high-speed signals. The important performance parameters are the dielectric constant of the material and the wiring density that can be achieved with. it. Fig. 3 shows how the dielectric constant and wiring density have evolved over the last five decades.

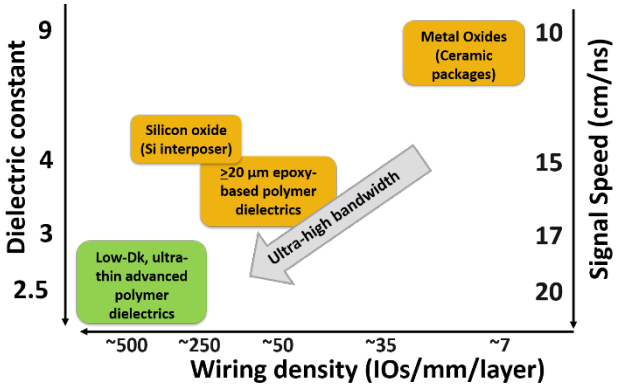

Figure 3. Evolution of low dielectric constant and high wiring density RDL technologies

Georgia Tech has been developing polymer RDLs on glass capable of supporting ultra-high wiring densities with advanced. And ultra-thin polymer dielectric materials, processes and lithography. Dielectric materials for this application can be classified as photoimageable or non-photoimageable. The Georgia Tech team has demonstrated panel substrates with 2 µm lines and spaces by advanced semi-additive processes (SAP) using non -photoimageable, dry-film dielectrics, as shown in fig. 3. To address the traditional limitations of SAP in pitch scaling, a novel via-in-trench (VIT) and via-in-line (VIL) embedded trench+via methods have been conceived and demonstrated to achieve ultra-fine pitch RDL on large panels, as shown in Fig. 4. with < 7 µm dia.microvias in ultra-thin dielectrics using a UV laser tool thus demonstrating silicon-like RDL on glass panels with advanced low-D_k dielectric materials and SAP processes.

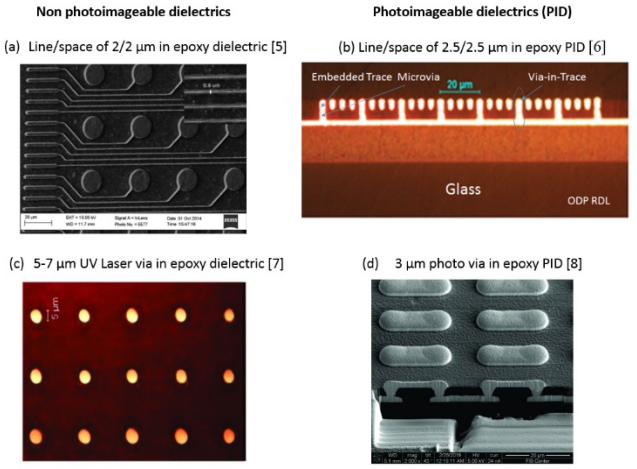

Figure 4. Advanced RDL dielectric materials and SAP processes for 2 µm RDL on glass panels

GLASS PANEL LITHOGRAPHY TO 1 MICROMETER

RDL wiring on wafers has been sub-micron for decades. This technology, previously employed for BEOL on chips, has finally moved for off-chip packaging onto silicon interposers. Recent product announcements such as by Intel's EMIB, TSMC's InFO, and AMD Fiji GPU are all operating on this technology [9]. This strategy, however, is a short-term solution as the data rate per channel is limited to speeds between 2-4 Gb/s and even silicon end-users are demanding more [10-11]. Georgia Tech's strategy to overcome this challenge involves many approaches. One approach involves lowering the resistance of RDL by innovations in lithography tools for numerical aperture and depth of focus, and in SAP processes with high aspect ratio conductors, as shown in Fig. 5.

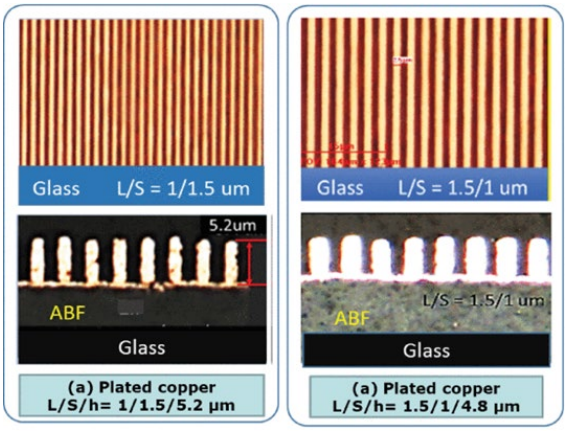

Figure 5. Next Generation High Aspect Ratio 1µm RDL for HPC Developed at Georgia Tech [11]

GLASS PANEL EMBEDDING (GPE)

Embedded Wafer Level Fan Out (WLFO) packages have disrupted the entire semiconductor industry due to their benefits in size, cost, electrical performance and potential for heterogeneous integration. Although they were initially designed to extend package I/O counts beyond fan-in Wafer Level Packages (WLP), the scope of WLFO technology has expanded significantly in recent years to include multi-die SiP modules with high-density RDL, as well as high I/O logic and memory integrations. Most WLFO packaging technologies today use epoxy-based mold compounds as the carrier [12]. These limit the wafer fan out packages in many ways that include lower wiring density due to die shift, higher warpage and higher electrical loss. Georgia Tech has been developing all the key technologies necessary to address these challenges by its glass panel embedding (GPE) [13].

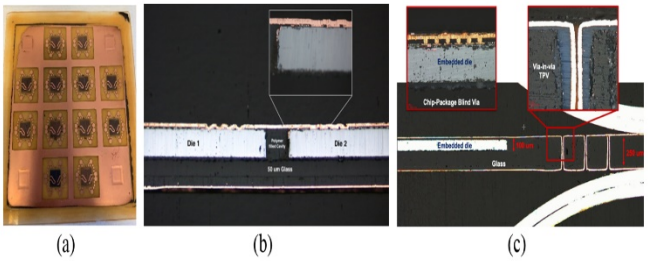

Figure 6. (a) 2 Metal-layer GPE on 100x100mm Panel (b) 2.5D GPE with multi-die embedded in glass cavities (c) 3D GPE with TPV integration

Glass, when used as a substrate for die embedding, provides many benefits, not found in existing WLFO technologies. The smooth surface and high-dimensional stability of glass enables silicon-like RDL wiring and BEOL-like I/Os even on large panels, with an unparalleled combination of ultra- high I/Os and lower cost. The CTE of glass can be tailored thus enabling the direct attach to board. Glass has ~2-3X lower loss-tangent as compared to most mold compounds, making GPE a better candidate for high-frequency applications. Glass also provides high resistivity, excellent moisture resistance, and high surface smoothness, compared to mold compounds.

GPE packages offer < 2 µm die-shifts, enabling chip-first, multi-die, high density 2.5D packages, as shown in Figure 6. (a) 2 Metal-layer GPE on 100x100mm Panel (b) 2.5D GPE with multi-die embedded in glass cavities (c) 3D GPE with TGV integration[13]. The lower die shifts imply the pad sizes necessary are smaller, significantly lowering the energy per bit. Dies can be placed side-by-side at < 100 µm distances, allowing bandwidth densities > 1TBps. GPE technology has also been used to demonstrate 3D packages with ultra-short (< 50 µm) logic-to-memory interconnect lengths [14]. Through- glass- via (TGV) integration has also been demonstrated enabling double side metallization for applications like Antenna-in-Package (AiP) for 5G and beyond applications

THERMAL TECHNOLOGIES FOR GLASS PACKAGES

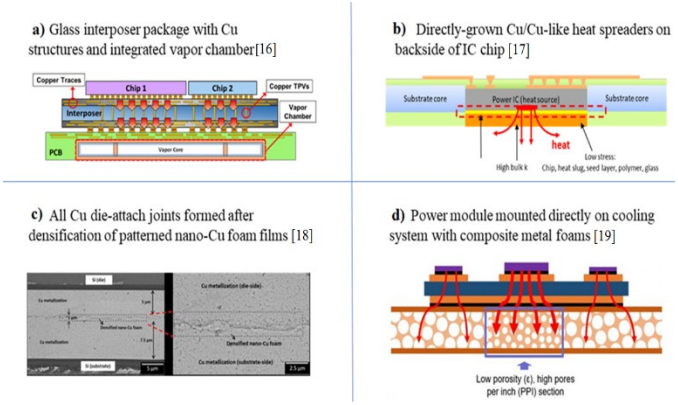

Figure 7. Georgia Tech's Approaches to Thermal Management in Glass Packages

Glass, although a better thermal conductor than organic laminates, it is a poor conductor compared to Si. The Georgia Tech team is comprehensively addressing the thermal challenges with glass packaging with many advances in thermal management at chip and system levels (16-19), as shown in Fig. 7. It proposed and demonstrated a novel substrate cooling approach to overcome the limitations associated with low thermal conductivity of glass by incorporating copper structures such as through-package vias (TPVs), copper slugs, and copper traces in redistribution layers (RDL) into glass substrates In addition, it integrated ultra-thin (< 1 mm) two-phase heat spreaders (vapor chambers) which can spread heat more efficiently than copper into the motherboard. The Georgia Tech team has also developed next-generation thermal interface materials (TIMs) for both embedded and substrate-based packages, aimed at reducing the thermal interface resistances to provide maximum heat transfer from the chip. In embedded packages, this approach involved direct-plated copper and copper-composites, resulting in near-zero thermal interface resistance [17]. In chip-last, substrate-based packages, an innovative sintering approach to form thin interfaces is also proposed and developed to realize all-Cu die-attach joints with minimum contact resistance and highest thermal and electrical conductivities to meet the emerging needs in high power systems.

SUMMARY

Glass packaging is emerging as next generation packaging platform beyond organic and silicon packaging. It has been developed in both chip first and chip-last 2.5D and 3D architectures. Georgia Tech and its industry partners have developed all the building block technologies necessary to manufacture. Currently two companies are making plans to manufacture in 2020.

REFERENCES

[1] Tummala Rao, et al. "Heterogeneous and homogeneous package integration technologies at device and system levels." 2018 Pan Pacific Microelectronics Symposium (Pan Pacific). IEEE, 2018.

[2] Lau John H, "3D Integration." Fan-Out Wafer-Level Packaging. Springer, Singapore, 2018. 231-268.

[3] Sawyer Brett et al., "Modeling, design, fabrication and characterization of first large 2.5 D glass interposer as a superior alternative to silicon and organic interposers at 50 micron bump pitch." 2014 IEEE 64th Electronic Components and Technology Conference (ECTC). IEEE, 2014.

[4] Ravichandran Siddharth et al., "Low-Cost Non-TSV Based 3D Packaging Using Glass Panel Embedding (GPE) for Power-Efficient, High-Bandwidth Heterogeneous Integration." 2019 IEEE 69th Electronic Components and Technology Conference (ECTC). IEEE, 2019.

[5] H. Lu et al., "Design, Modeling, Fabrication and Characterization of 2–5um Redistribution Layer Traces by Advanced Semi-additive Processes on Low-Cost Panel-Based Glass Interposers," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 6, no. 6, pp. 959-967, 2016.

[6] F. Liu et al., "Organic Damascene Process for 1.5um Panel-Scale Redistribution Layer Technology Using 5um-Thick Dry Film Photosensitive Dielectrics," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 8, no. 5, pp. 792-801, 2018.

[7] F. Liu et al., "Next Generation of 2-7 Micron Ultra-Small Microvias for 2.5 D Panel Redistribution Layer by Using Laser and Photolithography Technologies," in 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), 2019, pp. 924-930: IEEE.

[8] D. Okamoto et al., "Fabrication and Reliability Demonstration of 3 µm Diameter Photo Vias at 15 µm Pitch in Thin Photosensitive Dielectric Dry Film for 2.5 D Glass Interposer Applications," in 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), 2019, pp. 2112-2116: IEEE.

[9] R. Mahajan et al., "Embedded multi-die interconnect bridge (EMIB)—A high density high bandwidth packaging interconnect", Proc. IEEE 66th Electron. Compon. Technol. Conf. (ECTC), pp. 557-565, May/Jun. 2016.

[10] B. Sabi, "Advanced packaging in the new world of data", Proc. IEEE 67th Electron. Compon. Technol. Conf., May 2017

[11] Liu Fuhan, et al. "Low Cost 1μm Photolithography Technologies for Large-Body-Size, Low-Resistance Panel-Based RDL." Transactions on Components, Packaging and Manufacturing Technology (CPMT). IEEE, 2019
[12] C. F. Tseng, C. S. Liu, C. H. Wu, and D. Yu, "InFO (Wafer Level Integrated Fan-Out) Technology," Proc.-Electron. Components Technol. Conf., vol. 2016–August, pp. 1–6, 2016.
[13] Ravichandran, Siddharth, et al. "2.5 D Glass Panel Embedded (GPE) Packages with Better I/O Density, Performance, Cost and Reliability than Current Silicon Interposers and High-Density Fan-Out Packages." 2018 IEEE 68th Electronic Components and Technology Conference (ECTC). IEEE, 2018.
[14] Ravichandran Siddharth et al. "Design and demonstration of Glass Panel Embedding for 3D System Packages for heterogeneous integration applications." Journal of Microelectronics and Electronic Packaging 16.3 (2019): 124-135.
[15] Tummala Rao et al., "Heterogeneous and homogeneous package integration technologies at device and system levels." 2018 Pan Pacific Microelectronics Symposium (Pan Pacific). IEEE, 2018
[16] Broughton, J. et al., "Thermal management of power electronics using stochastic, open-cell metal foams." 2019 25th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC). IEEE, 2019.
[17] Nedumthakady Nithin et al., "Integrated Copper Heat Spreaders in Glass Panel Embedded Packages with Near-Zero Thermal Interface Resistance." 2018 IEEE 68th Electronic Components and Technology Conference (ECTC). IEEE, 2018.
[18] Mohan, Kashyap et al., "Low-temperature, organics-free sintering of nanoporous copper for reliable, high-temperature and high-power die-attach interconnections." 2017 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, 2017.
[19] Li Yongtong et al., "Thermal performance analysis of biporous metal foam heat sink." Journal of Heat Transfer 139.5 (2017): 052005.