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Cleanliness of Stencils and Cleaned Misprinted Circuit Boards

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The effectiveness of cleaning stencils and misprinted/dirty printed circuit boards can be effectively monitored. This can be done by washing known clean circuit boards and then checking to see if they have stayed clean as a result of the washing process. The monitoring can be done with conductivity equipment. Control limits can be set once enough initial data is collected. Correlations between machine maintenance and the volume of boards washed could be determined.

Introduction

There are long-established standards[1,2] and test methods[3] for ionic cleanliness levels for bare printed circuit boards and printed circuit packs. There is experimental data about component cleanliness[4,5], but no publically available standards known to the author. What about stencils, specifically stencils that are being used, cleaned and reused, as opposed to brand new stencils right out of the supplier's box?

This could be an issue for at least three reasons. If the stencil is not properly cleaned, then any obstruction in the apertures could lead to an improper amount of solder paste being deposited in that particular hole in the stencil. This could lead to an open or at least a smaller, potentially weaker solder joint. Even if it would not actually cause a reliability problem, it may be deemed unacceptable from a workmanship standard, leading to rework and the attendant possible effects this could have on long term circuit pack reliability.

Secondly, the material, most likely old solder paste, might actually get deposited with the new solder paste. The older material might be solder rich or solder poor or "crusty" and any of these three sub-cases could cause problems. The first could mean that there might not be enough flux to remove all the extra oxide. The second could lead to too small a solder fillet, as discussed above. The third case might mean a mixed obstruction inside the solder joint that does not break up, leading to stress concentration points in the solidified joint.

Less likely, if stencils are cleaned with a dirty cloth or in a cleaning apparatus with dirty solvent, then potentially the stencil could have a thin layer of highly ionic material that might be dissolved in solder paste applied to the stencil and then be transferred to the circuit boards pasted with the stencil in question. This paper explains how stencil cleanliness can be monitored, provides results of such work and offers some observations on the method and results.

In a similar fashion, this paper gives parallel information about OSP boards after washing. When a company does not have an in-line or batch cleaner for regular production, it can be a challenge to figure out how to deal with situations where boards must be cleaned. Often there will be little in-house history or knowledge of how to solve the problem. Most likely the requirement to clean bare boards will be because of misprinting, but could also be due to boards printed but unable to be further processed because of a line down situation that lasted longer than the open time of the solder paste or because of other contamination of the boards. This latter situation could be a result of events in transportation, inadvertent finger prints detected before reflow or a spill of some sort on to the boards in the plant.

The objects being cleaned in this study are not uncomplicated metal parts with relatively large holes in them. Traditionally many circuit boards have been 62 mil thick, whereas stencils are often 5 to 8 mils thick. This certainly makes the holes in a circuit board harder to clean because of more unfavorable aspect ratios. Circuit boards also have rougher edges that can hold contaminates.

Chemically an FR-4 circuit board usually consists of borosilicate glass fibers; silane coupler; a two-part epoxy resin; copper; solder mask and some kind of final finish for the plated through holes, outside vias and pads. Many processes in making a circuit board use ionic halogen-containing materials. There is essentially no way that a solid material that contains organically bonded halogens (chlorine and bromine in this context) that is subjected to processes which could be construed as being up to "medium aggressive" in nature will not release some of the chloride or bromide present. The two main sources from the original board manufacture will be miniscule amounts of unreacted tetrabromobisphenol A and plating solutions. Additional sources could be HASL fluxes and some solder masks. For the newer halogen-free circuit boards, the potential for free bromide from unreacted starting material and from broken carbon-bromine bonds of the polymerized resin is replaced by the possibility of free hydroxide being liberated from incompletely encapsulated magnesium and/or aluminum hydroxides.

All this should lead one to understand that the ionic cleanliness readings for bare circuit boards will not be as low as those for stencils, irrespective of cleaning agent and cleaning apparatus.

Experimental

Eight bare test boards originally manufactured for other end uses were chosen to be used to check the cleaning ability of the two cleaning systems, five for the stencil washer and three for the circuit board cleaner. The boards were made of FR4, 16.85 mm x 11 mm x 62 mil in dimensions, with 46 plated through holes. See **Figure 1**.

The boards and a holder for immersing them into the stencil cleaner were cleaned in a calibrated Alpha Metals Ionograph 500M SMD II to a level of 185 M-Ωcm or better. The Ionograph was filled with a 75:25 IPA:DI water mixed. The machine was run at a temperature of 25C. The boards were always handled with clean tongs or clean latex gloves.

The sample frame and the boards (**Figure 2**) were then put in the stencil washer, a Smart Sonic Model 6000. The wash solution was the aqueous-based Smart Sonic 440R. After a normal wash cycle, the holder and boards were removed and the cleanliness of the bare boards was checked by again using the Ionograph.

To check the ECM Global Technologies Inc. Cyber Clean 1000, Model 16PC board washer, the three Iongraph pre-cleaned boards were washed in isopropyl alcohol in the Model 16PC for the proscribed length of time and then dried. Subsequently they were checked for cleanliness in the Ionograph.

Results

Stencil Cleaning

Testing of the stencil washer commenced the 18th work week of 2007 and has generally been carried out every week thereafter. In summary, the number of measurements/number of weeks ratios for 2007, 2008 and 2009 (up to the time the paper was written) are: 25/35, 59/53 and 47/27, respectively. As one can see, the frequency of measure has increased year over year. The average values and standard deviations are shown in **Table 1**, excluding the aberration after week 16 of this year. The actual measurement data are graphed in **Figures 3-5**. The average value appears to have settled at 0.015 ug NaCl equivalent per square centimeter, double what it was for 2007.

Major preventative maintenance (PM) activities for the stencil cleaner include annual and semi-annual maintenance and "evaporator maintenance". Completion of a PM of the cleaning machine did not always correlate with a decrease in measured sodium ion equivalents per square centimeter. The next step in the analysis was to examine the timing and effects of the monthly maintenances. The correlation was even worse.

Table 1 Average Yearly Cleanliness Readings for Cleaned Stencils

Year	ug NaCl equivalent
2007	0.0072 +/- 0.0060
2008	0.015 +/- 0.013
2009	0.015 +/- 0.012

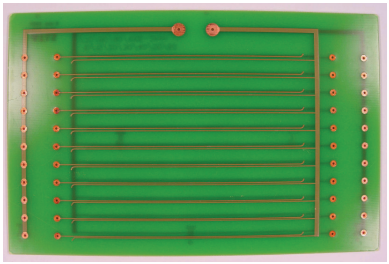

Figure 1 Bare Board Used to Test for Cleanliness

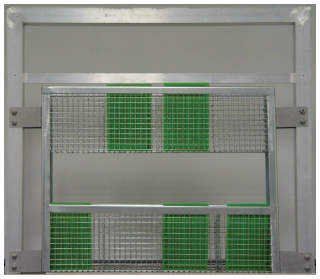

Figure 2 Holder for Bare Board Used to Test for Cleanliness

No records were kept of the number of stencils washed per unit time that would allow an attempt to make the correlation between conductivity results and the volume of washed stencils. And of course the amount of solder paste left on the stencils would differ depending on how diligent employees were in removing the solder paste remaining on the stencil after use in the printer. And finally the reasons for no correlation between measured conductivity values and PMs are augmented by the discovery that a sludge could gather in one part of the machine that was not removed by anything but the most thorough cleaning. This came to light during the unusually high readings during the latter half of April of this year.

It should be pointed out that other than the one time mentioned above, no reading has been higher than 0.07 ug/cm^2. This is well below the industry standard[1,2] for bare boards of 1 ug/cm^2. However, obviously the weakness of the detailed usefulness this value is that it is an average value and does not take into account local, high level concentrations of contaminates on a specific area of a board or stencil.

There are now enough data points that an upper control limit has been set for the process. See **Figure 6**. This value is 0.045 µg/cm^2. This value was set excluding the two unusual values noted above. With this control limit there were only 5 points above the control limit, including the two unusual ones. With the increased level and thoroughness of the preventative maintenance now being performed on the equipment, there should be few, if any, instances of measurements above the upper control limit.

Dirty Bare Board/Misprinted Board Cleaning

Not surprisingly these values are inherently higher than for stencils, for reasons pointed out in the Introduction. Like the data for the stencil washing, there was one episode where things were very bad. This happened in August of last year. Since that time the frequency of PMs for the machine and the change-out of the cleaning fluid has been increased. The cleanliness readings for 2009 have essentially been better by a factor of two. See **Figures 7 and 8**. Note the difference in y-axis scales.

It should be noted that the average conductivity value for 2009 (0.06 +/- 0.07 ug/cm^2) is about half that of 2008 (0.16 +/- 0.12 ug/cm^2, excluding the six points above 0.55). This is most likely the result of doubling the number of times per unit time that the filters are changed in the machine.

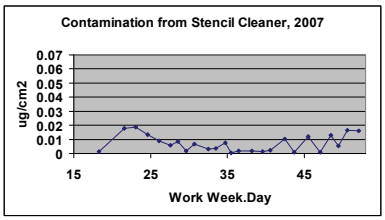

Figure 3 Stencil Cleanliness, 2007

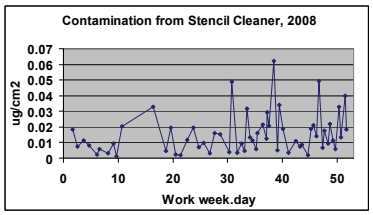

Figure 4 Stencil Cleanliness, 2008

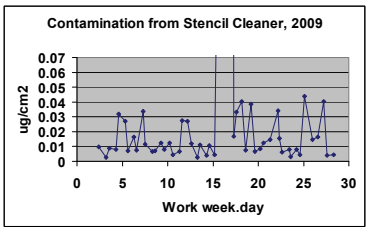

Figure 5 Stencil Cleanliness, 2009

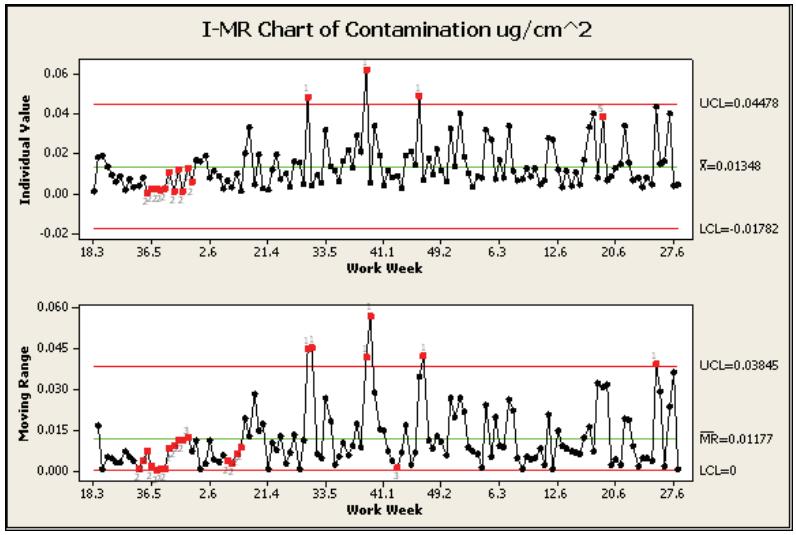

Figure 6 Stencil Cleanliness Data with Calculated Control Limits

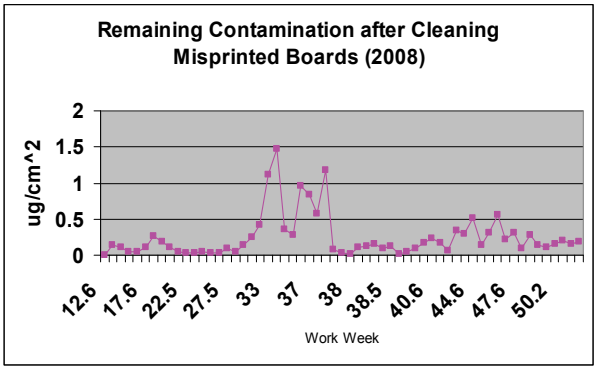

Figure 7 Board Cleanliness after Cleaning, 2008

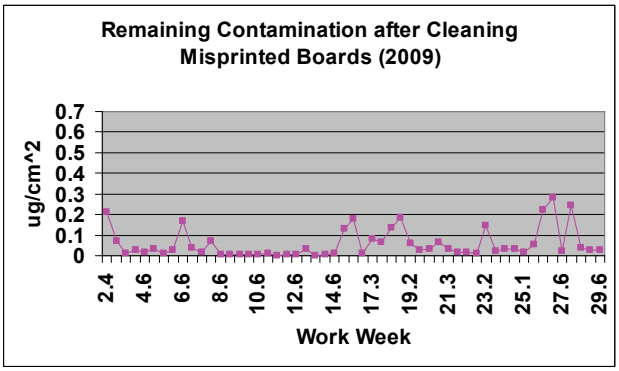

Figure 8 Board Cleanliness after Cleaning, 2009

Access to data on the number of boards washed per unit of time allowed the attempt to find correlations between this and the readings. Conductivity values are also larger than the range that could arguably be considered almost "noise" for most of the stencil readings. Rough correlations to both the number of boards washed and the major PMs of the machine have been made. **Figure 9** is a plot of both the number of boards washed and the cleanliness values and one can see that the broad peak in the number of washed boards centered around weeks 40-50 of last year corresponds to the high conductivity values of the boards cleaned at that time.

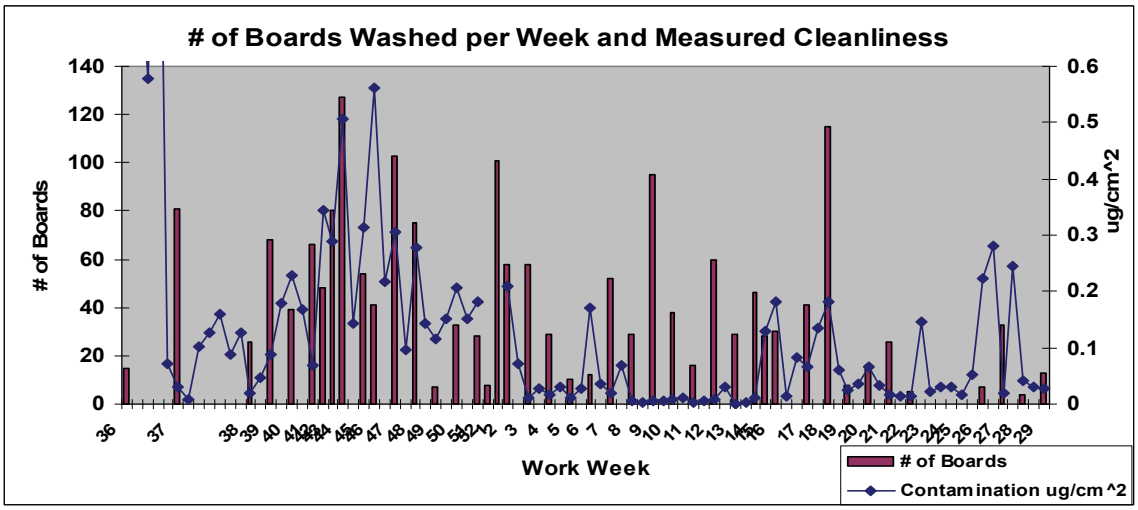

Figure 9 Showing Rough Correlation between Number of Boards Washed and Cleanliness Values Recorded

And finally, excluding the five high points of last August, the data has been used to determine an upper control limit for the board cleaning (**Figure 10**). That value is 0.30 µg/cm^2. The number of total points above that limit is 5.

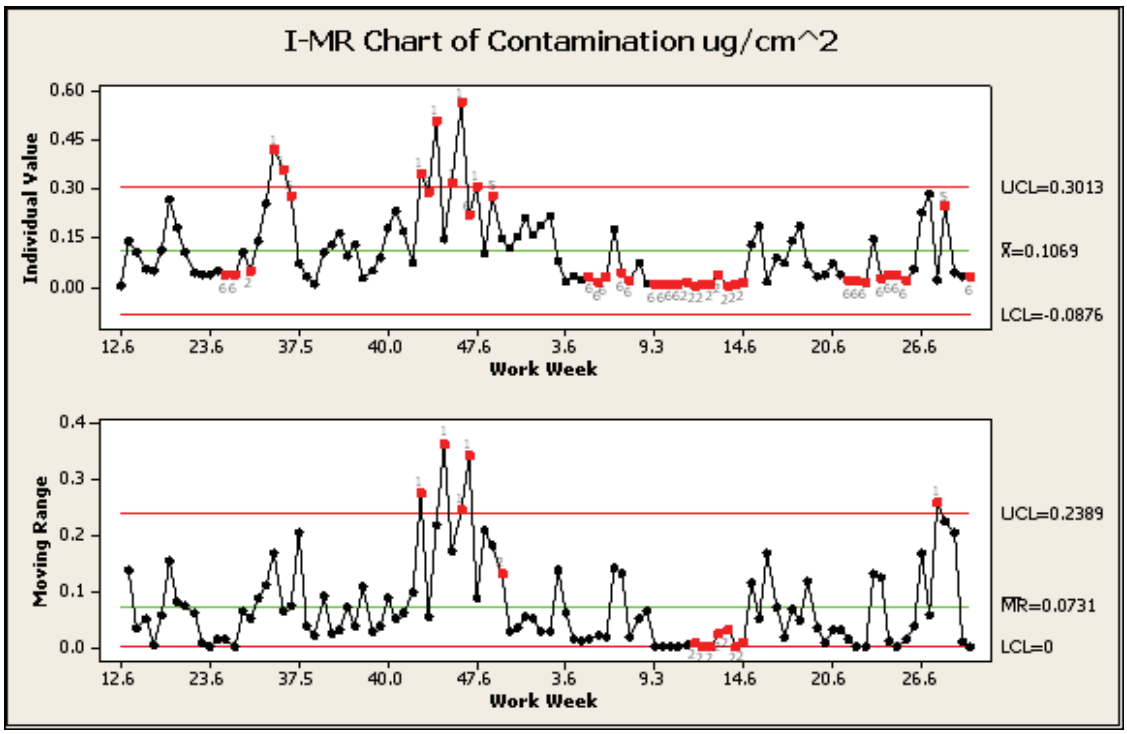

Figure 10 Board Cleanliness Data with Calculated Control Limits

Conclusions

Control of a stencil cleaner's cleaning ability is possible, but requires assiduous discipline in maintaining a preventative maintenance program. Examination and cleaning of unusual dead spots in the machine is required to avoid the buildup of residues from which ionic material can later leach out. Since most facilities that do any kind of circuit pack washing will already have a conductivity apparatus for measuring the efficiency of their in-line or batch cleaner for regular production, this monitoring program would not be hard to add. For an installation that is essentially no-clean, this would require either buying a full-size piece of equipment or at least some beakers and a conductivity probe to be used with smaller boards that could be the test pieces. It must be admitted that the negative consequences of not putting this type of program in place are quite small.

However, the stakes are much higher with regards to dirty circuit boards. Often rework, whether cleaning misprinted boards or work involving hand soldering, etc. is considered as "out of sight out of mind". But even in the best facilities "things happen", to put it mildly. Every company should have some way of monitoring the cleanliness of all board types that are used to build product for their customers.

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