BOARD LEVEL RELIABILITY COMPARISON OF BGA AND LGA PACKAGES MOUNTED TO AN LGA FOOTPRINT MOTHERBOARD

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ABSTRACT
The present study compares board level reliability of both BGA and LGA packages mounted to motherboards with an LGA footprint. SMT yield, drop test performance, and thermal cycle performance were evaluated. Finite element analysis was also used to compare with the measured reliability testing. Both the BGA and LGA devices self-align well without open, shorted, or inconsistent solder joints. The package can be displaced off the pad by no more than 0.200mm, and solder paste misprinting must be limited to 0.050mm. There were no confirmed failures in solder joints up to 3042 temperature cycles. Simulation predicts that the LGA package should have 1.5X longer fatigue life than the BGA package due to a larger perimeter I/O pads, and additional ground pads in the interior of the module. There were no failures in drop testing up to 400 cycles. Overall, both modules showed excellent board level reliability that far exceeds typical consumer product requirements.

Key words: LGA, BGA, SMT, BLR

INTRODUCTION
Laminate based RF modules for wireless applications typically have relatively small body size (<8mm) and LGA style package terminals. In some applications, BGA style packages are being evaluated as a way of populating both sides of the module substrate. It is most convenient for product flexibility if both LGA and BGA style packages can be used on the same motherboard footprint.

The present study compares board level reliability of both BGA and LGA packages mounted to motherboards with an LGA footprint. SMT yield, drop test performance, and thermal cycle performance were evaluated. Finite element analysis was also used to better understand reliability performance.

TEST BOARD ASSEMBLY
Standard surface mount materials and processes were used to mount the subject packages to the test boards including lead-free solder paste, stencil print, pick and place of components, convection reflow soldering, and visual and X-ray inspections.

Components
Two types of packages and one test board comprised the test materials for this evaluation. The packages were a 3x5 mm size LGA and a BGA version of the same device. The LGA (Figure 1) had a 8x5 matrix of 0.3x0.4mm size pads on a pitch of 0.650mm with (3) 0.9x1.3mm e-pads in the center. The BGA package (Figure 2) had the same pitch and matrix, but used 0.35mm dia. SAC balls for I/O soldering connections.

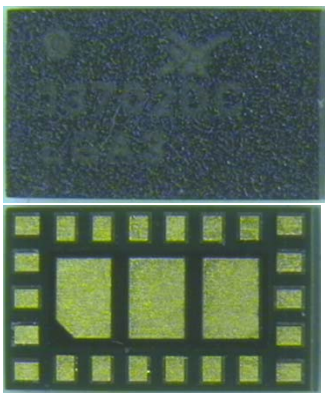


Figure 1: LGA Package

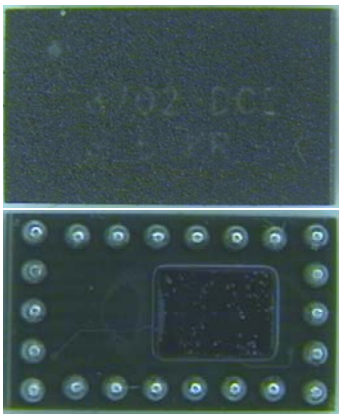


Figure 2: BGA Package

Test Board

The test board (Figure 3) was a 132x77x1mm, 8 layer FR-4 JEDEC design with Cu OSP finish that included 3x5 matrix of the LGA package (footprint) land pad design having 0.3x0.4mm non-solder mask defined (NSMD) I/O pads and (3) solder mask defined (SMD) 1x1.4mm openings which comprise the e-pad.

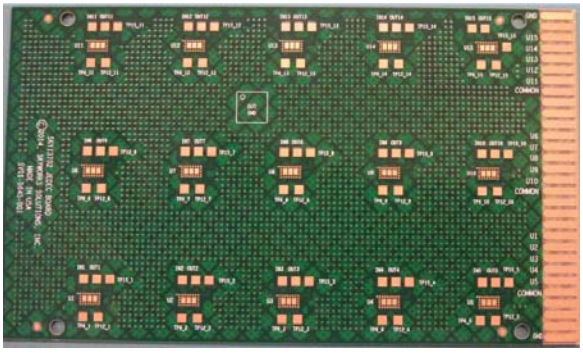


Figure 3: Test board with LGA footprint and pads.

Stencil Design

The same stencil was used for both packages, and the design of its apertures reflected the LGA package pads and the test board with following features (Figure 4):

- Ni laser cut, 80um thick foil. Though a thicker stencil can work for typical SMT processes, a lower thickness stencil was used in this case to produce joints having less solder paste and tack strength and thereby testing the 'worst case' condition.
- I/O pad aperture 0.3x0.4mm (1:1 to PCB pad size), aspect ratio > 1.5 and area ratio > 0.66 (which was considered acceptable)
- E-pad apertures were modified to 2x3 array of 0.6x0.9mm at 0.1mm gap/space which reflected a ~20% reduction to test board pad

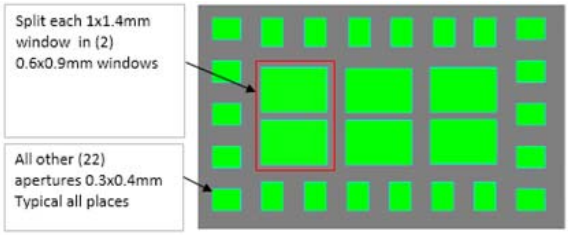


Figure 4: Stencil aperture design.

Solder Paste

A low residue, no-clean SAC 305, 88.5% metal loaded, type 4 paste was used for lower voiding, good rheology, and high transfer efficiency.

Solder Paste Print

Solder paste was printed using the same equipment and parameters for both packages (Table 1).

Table 1: Solder paste printing parameters

Printer Type	Automatic stencil printer
Squeegee	Metal, 60° angled
Print Speed	15mm/s
Print Pressure	6kg
Print Stroke	1
Separation Speed	3mm/s
Stencil Clean	Dry wipe and vacuum once every 5 boards
Printing Atmosphere	Temp: 23-25C, 38% RH,

Printed paste release and quality was acceptable and repeatable without any missing or bridged paste deposits. Height and volume of I/O pads were measured with SPI (solder paste inspection) equipment (Figure 5). The height and volume were within the expected range (0.100 + 0.025mm) but slightly on the high side. This is primarily due to the 0.020mm thick solder mask on the SMD e-pad acting as a stand-off. The transfer efficiency was slightly greater than 100% which is to be expected because of the larger aperture area ratio of the stencil.

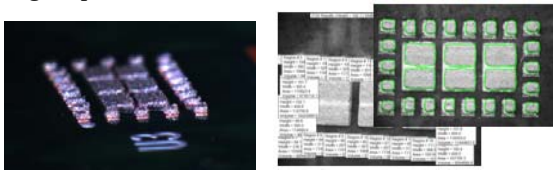


Figure 5: Solder paste measured with SPI equipment

- Height: Avg ~0.103mm (0.94 – 0.111mm)
- Volume: Avg ~0.0103mm3 (0.087 – 0.0107mm3)
- Transfer efficiency (volume): ~107% (91% - 111%)

Component Placement

150 of each packages were mounted on test boards with pick and place equipment using vision to locate package outline with placement accuracy tolerance of 30µm or less

(± 3 sigma) and placement force of 1.5N (Figure 6). Both packages were pressed down into the printed solder paste for sufficient tack and best self-alignment.

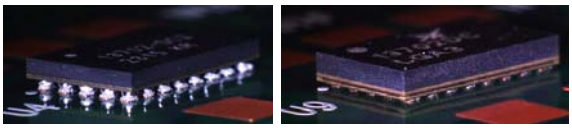


Figure 6: BGA and LGA rest on solder paste

Solder Reflow

All boards and parts were reflowed in a hot air convection oven using the same profile optimized to avoid excessive preheat and peak temperature (max 245°C) to help minimize voids (Figure 7).

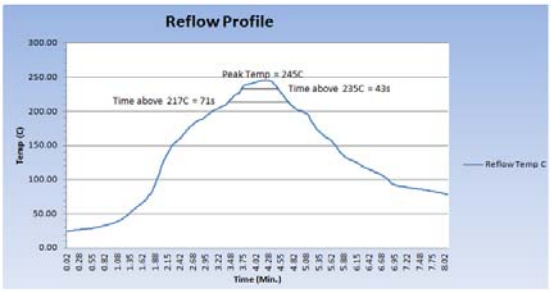


Figure 7: Lead-free reflow profile

SMT RESULTS

During and after assembly, no SMT process issues or challenges with either the LGA or BGA components were encountered. No failing or inconsistent solder joints were detected during visual and X-ray inspection (Figure 8), and all components were verified by electrical testing as described later herein. Both component styles exhibited good self-alignment after reflow. Voids were less than 25% of I/O pads and less than 20% on e-pads.

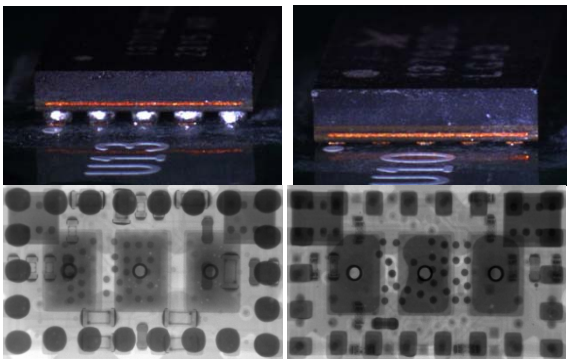


Figure 8: BGA and LGA visual and X-ray inspections

The average BGA solder joint stand-off was measured to be 0.206mm (0.190-0.212mm) where the LGA was only 0.048mm (0.021mm- 0.066mm) (Figure 9).

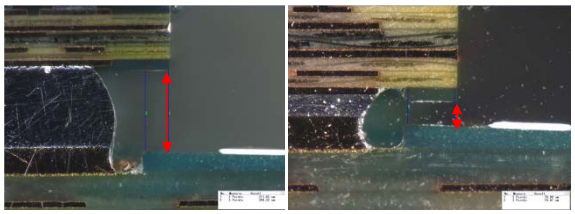


Figure 9: BGA and LGA solder joint stand-off

Self Alignment Evaluation of LGA vs. BGA

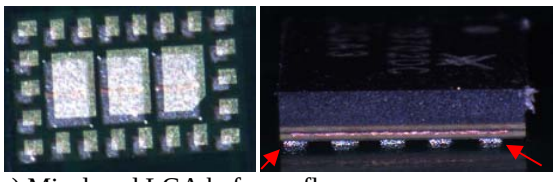
To investigate the robustness of the surface mount process associated with these package footprints, the effect of component misplacement and misprinted solder paste on self-alignment was evaluated (Table 2). Packages of each type (45) were intentionally misplaced by varying distances from their mating pads and misprinting was also performed on three boards.

Results showed that both the BGA and LGA devices self-align well without open, short or inconsistent solder joints, as long as the package is displaced off the pad by no more than 0.200mm and solder paste misprinting is limited to 0.050mm (in the direction opposite of the component misplacement). It was also noted that frequency of failed misalignment was higher in the LGA case than for BGA packages. Also, poor misalignment in the LGA case resulted in open and/or inconsistent solder joints whereas it created more solder shorts in the BGA case due to the larger volume of solder per joint (Figure 10).

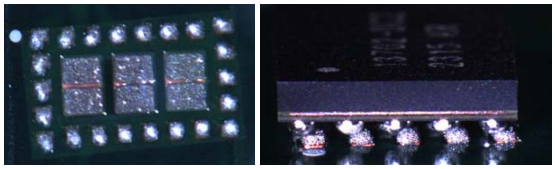
Table 2: Effect of component misplacement and misprint

Displacement (mm)	**LGA 0.100**	**LGA 0.150**	**LGA 0.200**
Print off 0.050	0/5	0/5	0/5
Print off 0.100	0/5	0/5	4/5
Print off 0.150	1/5	4/5	5/5

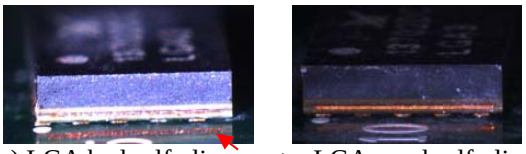
Displacement (mm)	**BGA 0.100**	**BGA 0.150**	**BGA 0.200**
Print off 0.050	0/5	0/5	0/5
Print off 0.100	0/5	0/5	2/5
Print off 0.150	0/5	2/5	5/5



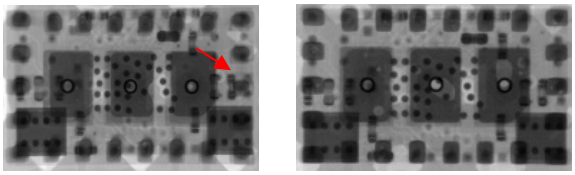
a) Misplaced LGA before reflow



b) Misplaced BGA before reflow

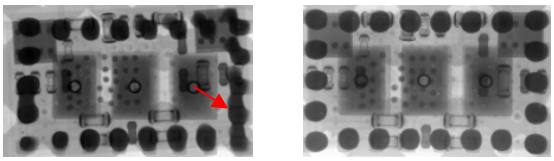


c) LGA bad self-alignment LGA good self-alignment



d) LGA inconsistent solder Joints LGA good solder joint

e) BGA failed self-alignment BGA self-aligned well



f) BGA shorts/inconsistent Joints (left) and good BGA solder joints (right)

Figure 10: LGA and BGA self-alignment and solder joint quality with intentional misplacement and misprint.

The misalignment/misprinting experiment performed here was conducted to simply explore the robustness of the surface mount process applied to these components. All the boards assembled for the purposes of temperature cycling and drop testing were produced using optimized, nominal conditions as reported at the beginning of this section.

THERMAL SHOCK TESTING

Initial Testing and Setup

After surface mount assembly of the packages to the test boards, the initial resistance of each device was measured to validate the time-zero electrical health of the entire population. All values measured were between 1.64 and 2.33 ohms. Summary statistics appear in Table 3 and Figure 11, which indicate satisfactory surface mounting results, and close agreement between package types (BGA and LGA).

Table 3: Time zero resistance statistics.

Board Type	Qty	Mean (Ohm)	StdDev (Ohm)
BGA	60	2.01	0.17
LGA	60	1.98	0.18

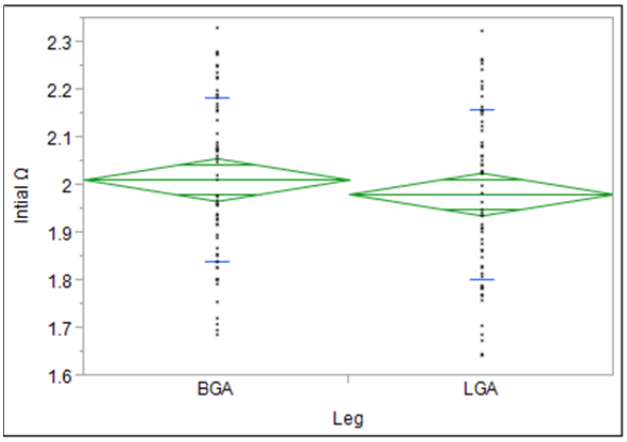


Figure 11: Device daisy chain resistance by joint type.

The variation in the initial resistance measurements is easily explained by trace length differences in the test board. Device resistances reported in Table 3 and Figure 11 are 2-wire measurements which include lead/trace resistance. When device resistances were grouped by "trace length", 1 being the shortest and 5 the longest, the data clearly demonstrate this effect as illustrated in Table 4 and Figure 12.

Table 4: Device resistance grouped by board location

Level	Qty	Mean (Ohm)	Std Dev (Ohm)
1	24	1.77	0.07
2	24	1.87	0.06
3	24	1.99	0.06
4	24	2.11	0.06
5	24	2.23	0.05

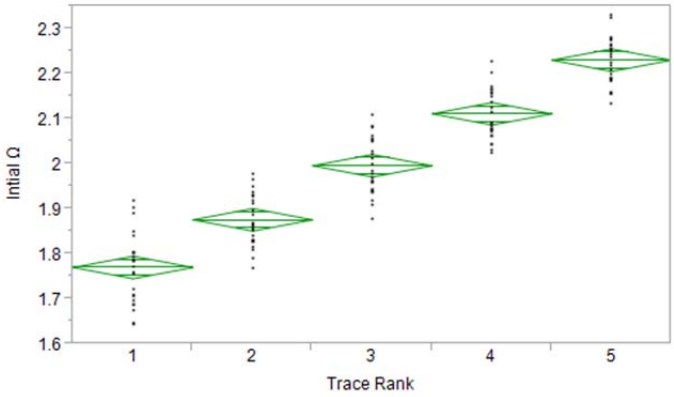


Figure 12: Device resistance grouped by board location

After the electrical characterization described above, connection to the boards was made using appropriate materials and hand soldered connections so as to avoid any issues with the temp cycling reliability of connectors. High-temperature ribbon cables were customized and attached to the board lands and ground pads were shorted together. This configuration is illustrated in Figure 13.

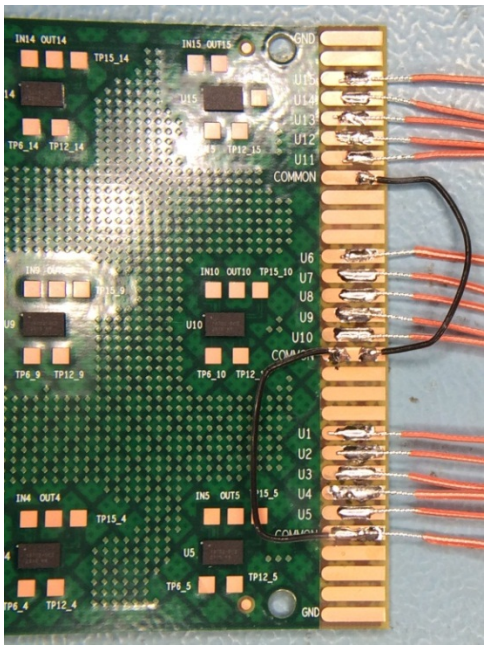


Figure 13: Daisy chained test board with hand soldered leads.

The other ends (the instrument connection end) of the test cables were terminated at a Keithley 3723-ST terminal panel (Figure 14). One advantage of this method is that correlation between the board device numbers, the cable conductors, the terminal block numbering, and the internal data channel is easily accomplished using a cross-reference table. This allows for simple subsequent manipulation of the data, and an example of a portion of the cross reference appears in Figure 15.

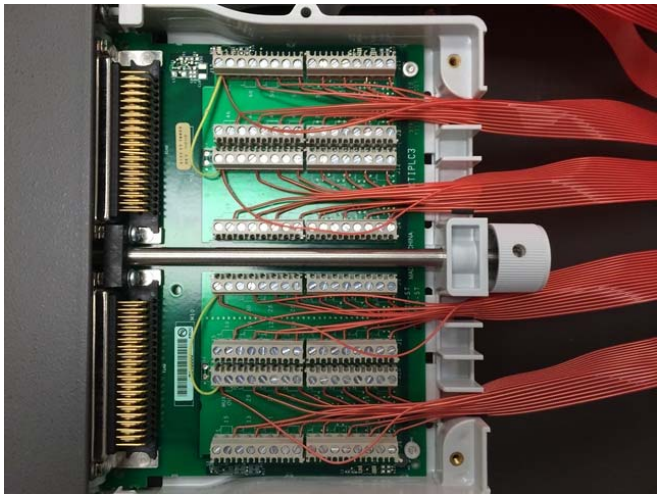


Figure 14: Keithley 3723-ST terminal panel

cable	conductor	Leg	Board	DUT	module	Channel	Intial Ω
1	1	BGA	1	U05	1	1001	1.6895
1	2	BGA	1	U04	1	1003	1.8425
1	3	BGA	1	U03	1	1005	1.9656
1	4	BGA	1	U02	1	1007	2.0804
1	5	BGA	1	U01	1	1009	2.2279
1	6	BGA	1	U10	1	1011	1.7012
1	7	BGA	1	U09	1	1013	1.8304
1	8	BGA	1	U08	1	1015	1.9433
1	10	BGA	1	U07	1	1029	2.0785
1	11	BGA	1	U06	1	1027	2.1927
1	12	BGA	1	U11	1	1025	2.2526
1	13	BGA	1	U12	1	1023	2.0927
1	14	BGA	1	U13	1	1021	1.9817
1	15	BGA	1	U14	1	1019	1.8591
1	16	BGA	1	U15	1	1017	1.8422
2	1	BGA	2	U05	1	1002	1.7121
2	2	BGA	2	U04	1	1004	1.8576
2	3	BGA	2	U03	1	1006	1.9611
2	4	BGA	2	U02	1	1008	2.0878
2	5	BGA	2	U01	1	1010	2.2016

Figure 15: Example of the cross reference table used to catalogue device resistance

The boards, cables, and thermocouples were then loaded into an Espec TSE-11A Thermal Shock System (Figure 16). This is a dual chamber system in which the sample area, or cage, moves on an elevator between two different hot and cold chamber zones. The airflow is from back to front in this particular case. Therefore, the boards are placed vertically and parallel to the air flow. Thermocouples were attached to the left-most and right-most boards.

The thermal shock chamber was programmed for 2 cycles per hour as follows: -40°C for 15 minutes, and +125°C for 15 minutes. Transfer of the substrate cage takes place in less than one minute, so the thermal transient itself in the boards/packages is dictated by the thermal mass involved. Temperature data were taken to confirm that the desired change in temperature was being achieved in the samples. Four cycles of such data are illustrated in Figure 17.

Figure 16: Cold chamber of the Espec TSE-11A.

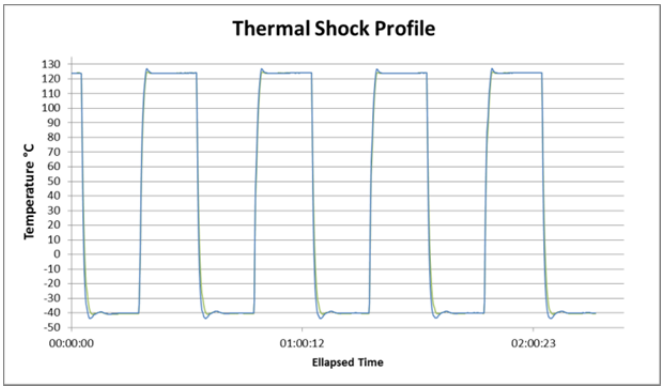


Figure 17: Thermal shock profile measured on test samples

Resistance of the packages was monitored at 3 minute intervals to ensure that values at both extreme temperatures are captured. Measurements were made using a Keithely 3706A Digital Multi-Meter.

THERMAL SHOCK RESULTS

As of 3042 cycles, only one device has failed and one other beginning to show a resistance increase. Both devices are from the LGA leg of the experiment.

Resistance Trends

The one failed device clearly demonstrates an electrical failure under stress as shown in Figures 18 and 19. Normal resistance changes due to temperature change are observed up to cycle number 1919 at which time the DUT resistance becomes large and erratic.

Failure Analysis

The failed device was extracted and cross-sectioned to examine all the perimeter solder joints. No clear and obvious crack was seen in any joint. One joint did show some damage near the intermetallic layer on the PCB side (Figures 20 and 21). It is not certain that this damage was the root cause of the resistance increase shown in Figures 18 and 19. Typically, a solder joint needs to be completely cracked to observe a 0.5Ohm increase in resistance.

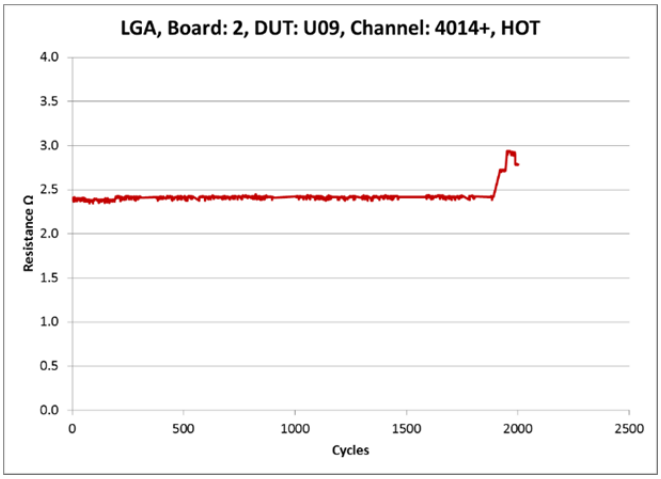


Figure 18: Sample resistance trend during the hot phase of the temperature shock cycles for failed unit.

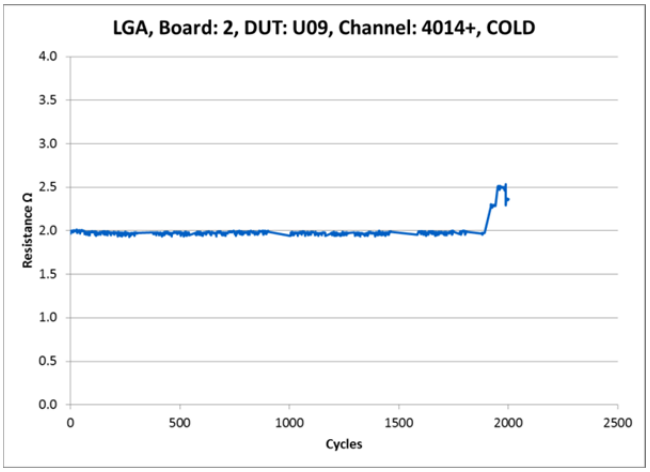


Figure 19: Sample resistance trend during the cold phase of the temperature shock cycles for failed unit

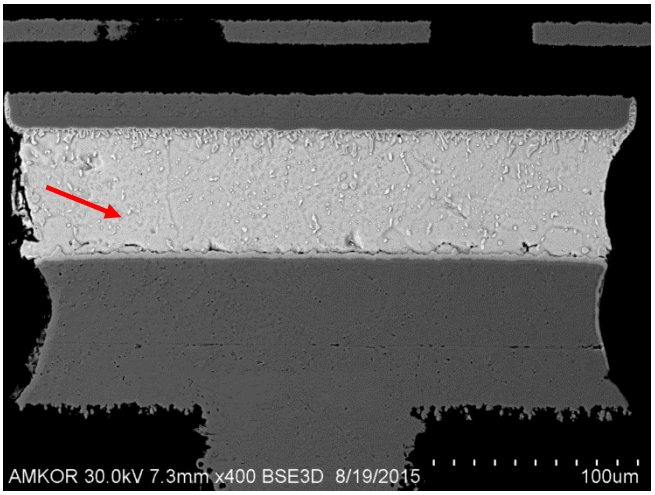


Figure 20: Worst case solder joint on failed unit showing some damage near intermetallic layer on PCB side of joint

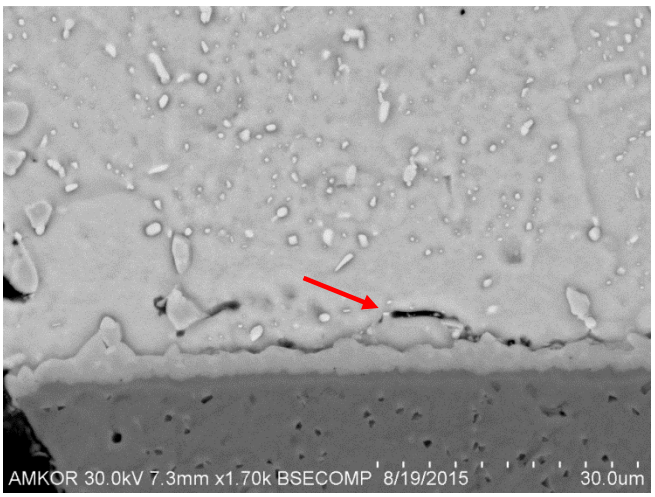


Figure 21: High magnification view of damaged region in Figure 20

FINITE ELEMENT ANALYSIS OF THERMAL SHOCK TEST

ANSYS finite element simulation was used to compare the predicted thermal cycling performance of the BGA and LGA packages. A quarter symmetric model was created to represent the geometry of the packages and was meshed using SOLID185 (brick), SOLID186 (tetrahedral) and VISCO107 elements (Figures 22 – 25). The smallest mesh size used for the solder joints is about 20um in-plane and 10um along the thickness of the joints.

The linear elastic material properties used for the model are shown in the Table 5. Multi-linear Isotropic Hardening properties was used for Copper from refs [1,2] and a SINH creep model was used for the SAC305 solder joint material from ref [3]. Creep simulation was performed over two thermal cycles starting at a stress free temperature of 125C. Each cycle is 30 minutes, with ramp times of 2 minutes, and dwell times of 13 minutes. A 20um thick layer of elements was used to calculate the volumetric average plastic strain energy density on the package side. A 30um thick layer was used on the mother board side.

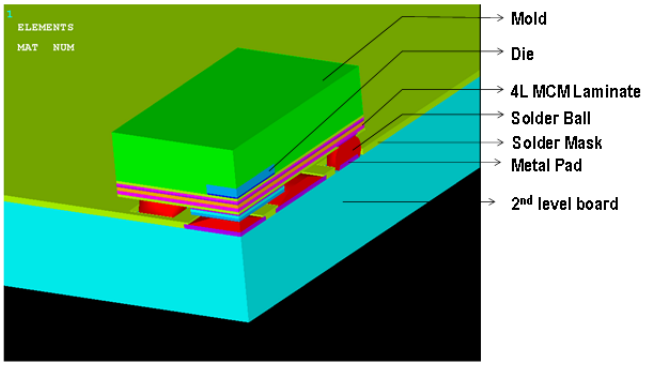


Figure 22: Quarter symmetry finite element model.

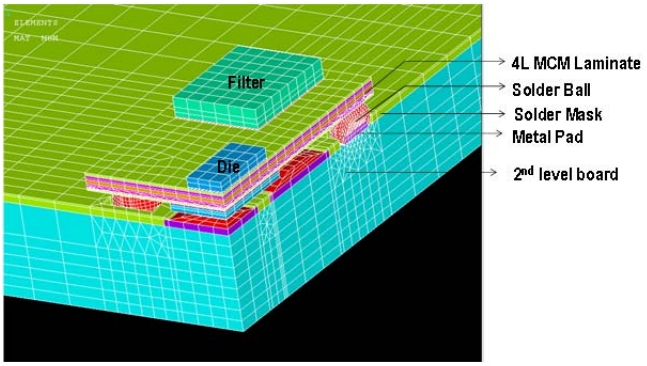


Figure 23: Mold cap removed showing die and passive component.

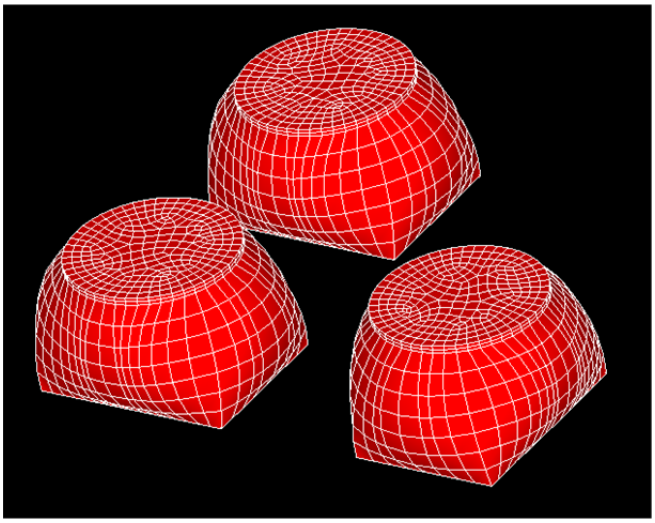


Figure 24: Detailed solder joint mesh for BGA joints.

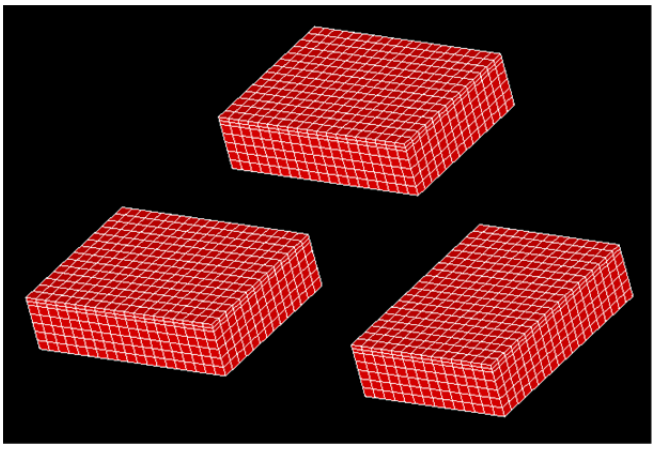


Figure 25: Detailed solder joint mesh for LGA joints.

Results showed that the accumulated viscoplastic strain energy density on the package side was much larger than on the mother board side of the joints (Figures 26 and 27). Also, the LGA package showed about 36% lower viscoplastic strain energy density per cycle than the BGA package. This was due to the 25% larger area of the perimeter LGA pads, and the additional support provided by the large center ground pads for the LGA package (which are not present in the BGA package).

Table 5: Linear elastic material properties.

Material	Young's Modulus (GPa)	Poisson's ratio	Tg (C)	Alpha 1 (ppm/C)	Alpha 2 (ppm/C)
GaAs	86	0.31	-	5.7	
Silicon	160	0.30	-	2.5	
Epoxy	12	0.30	100	20	70
Mold	27	0.25	130	8.0	32
MCM core	21	0.19	230	12 (x,y) 25.1 (z)	3.0 (x,y) 160 (z)
MCM build-up	13	0.19	230	15.1 (x,y) 29.6 (z)	6 (x,y) 184 (z)
Solder Mask	2.4	0.30	101	50	160
Ceramic Filter	300	0.23	-	8	
Copper (MISO)	124	0.34	-	17	
SAC305	42	0.40	-	22	
Mother Board	28	0.16	-	15 (x,y) 50 (z)	

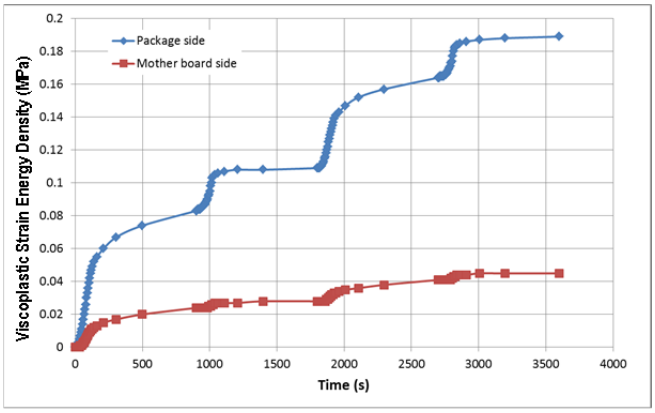


Figure 26: Accumulated strain energy density for BGA device.

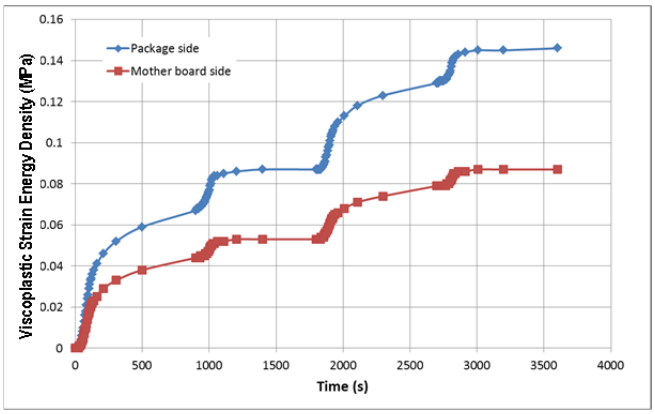


Figure 27: Accumulated strain energy density for LGA device.

Two different methods were used to calculate the predicted fatigue life based on the viscoplastic strain energy density per cycle. As shown in Table 6, using the direct calculation method, the first failure was predicted to be 2785 cycles for the BGA package and 3976 cycles for the LGA package. Using a crack initiation and growth methodology, the first failure was predicted to be 4284 cycles for the BGA package and 7106 cycles for the LGA package. At the time of this publication, only 3042 cycles had elapsed, and there was only one un-confirmed failure on the LGA package, so it is difficult to tell which method will end up closer to the measured results.

Table 6: Predicted fatigue life based on Ref [4]

	Direct Calculation		Crack Initiation and Growth			
	Ref [4], Table 7		Ref [4], Table 11			
	C1 (cycles)	C2	C1 (cycles)	C2	C3 (um/cycle)	C4
	145	-1.17	6	-1.43	1.49	1.14
	SED/cycle (Mpa)	First Failure (cycles)	a (um)	No (cycles)	da/dN (um/cycle)	First Failure (cycles)
BGA	0.080	2785	340	222	0.0837	4284
LGA	0.059	3976	400	343	0.0592	7106

DROP TEST

Second level drop test was performed on the LGA and BGA packages as per JEDEC JESD22-B111 standard. A total of 60units (4 boards x 15 units per board) were tested for each package type. A populated test board is shown in Fig 28. The board was secured to the base plate of the drop table with screws and washers using the four corner holes. A peak impact acceleration of 1500G shaped approximately like a half-sine waveform and lasting for 0.5ms was used. The measured acceleration profile is shown in Fig 29. An event detector was used to detect any resistance greater than 1000Ohms lasting for 1microseond or longer. Failure is defined as the first event of such intermittent discontinuity and followed by 3 additional such events during 5 subsequent drops.

Even after 400 drops none of the 60 LGA units or the 60 BGA units showed any failures.

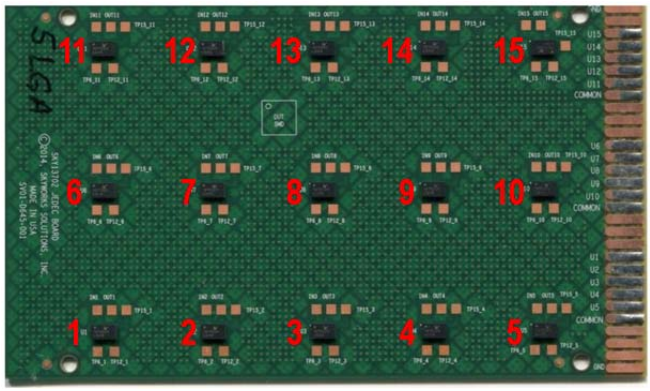


Figure 28: Drop test board with units mounted.

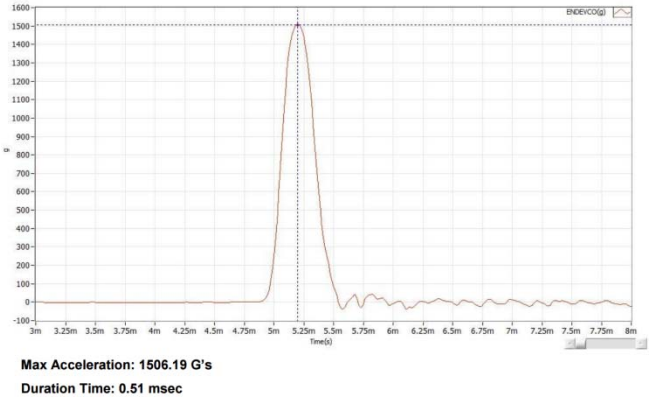


Figure 29: Drop test acceleration profile

CONCLUSIONS

1) Both the BGA and LGA devices self-align well without open, shorted or inconsistent solder joints. The maximum allowable displacement off the pad is 0.200mm, and solder paste misprinting must be limited to 0.050mm.
2) There were no confirmed failures in solder joints up to 3042 temperature cycles.
3) Simulation predicts that the LGA package should have 1.5X longer fatigue life than the BGA package due to a larger perimeter I/O pads, and additional ground pads in the interior of the module.
4) There were no failures in drop testing up to 400 drop cycles.
5) Overall, both modules showed excellent board level reliability that far exceeds typical consumer product requirements.

REFERENCES

1] CINDAS Report 105, Purdue University, December 1992.
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