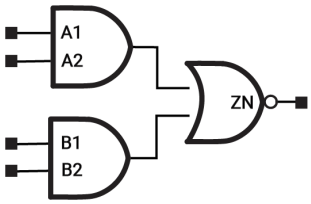
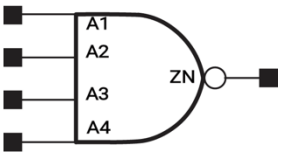
Agile Analog launches new Digital Standard Cell Library

Cambridge, UK 21, Sept, 2022. Agile Analog™, the analog IP innovators, has launched its Digital Standard Cell Library (DSCL). It provides a comprehensive library of digital cells enabling designers to implement the digital circuits required to control analog blocks in mixed signal solutions. The new digital library is available in thick-oxide based cells, operating above the core voltage domain, minimizing leakage and allowing easy migration across different process nodes even in FINFET technologies.



AND-OR

Barry Paterson, Agile Analog's CEO, explained, "The Agile DSCL has been developed to enable our customers to embed digital functionality within the analog domain. These digital cells will operate within the analog voltage domain which avoids excessive level shifting to the core domain and enables digital control to be tightly coupled to analog IP. The DSCL has been developed to be process agnostic and therefore is available in the same processes as our analog IP. The library fully supports industry standard digital design methodologies by making all required views available. Our Analog Digital Cell Library is already being used successfully in customer designs to support low power, always-on solutions for applications such as IoT."



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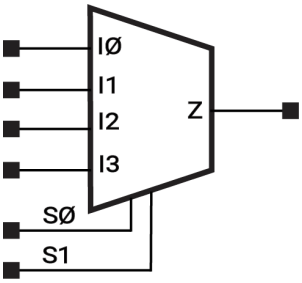
The DSCL IP blocks can be optimised for low-power, ultra-low leakage, high density or high-speed applications. There are options for channel length and various track heights to provide flexibility for designers. For specific design targets such as low-power designs, there is a special Power Management library. The library can be optimised for other PPA targets to ensure that customers have the best solution for their application. It is also possible to generate models at customised PVT corners. The library has class-leading verification and is DFM-optimised.



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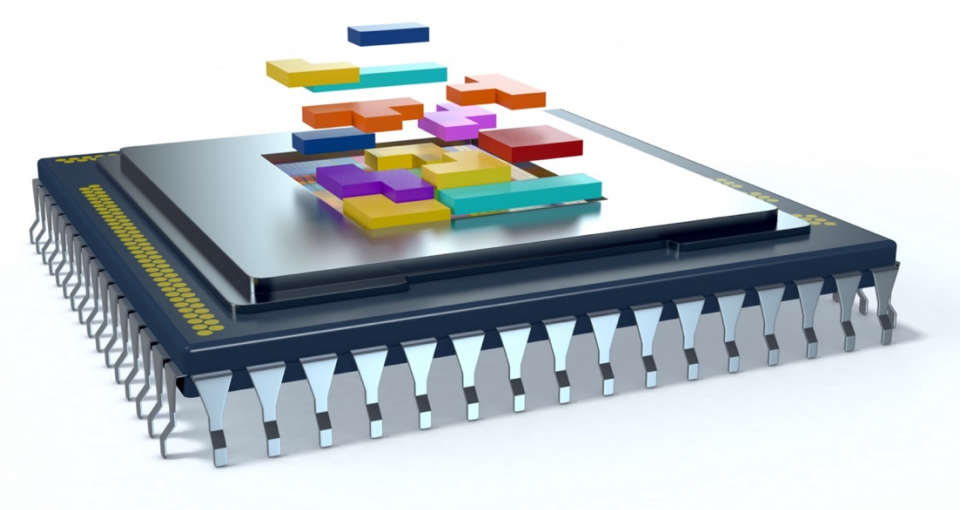

***Composa*™**
Traditionally, analog IP blocks have to be manually redesigned for each application and process technology but Agile Analog has a unique way to automatically generate analog IP to exactly meet the customer's specifications and process technology. Called Composa™, it uses tried and tested analog IP circuits that are in the company's Composa library. Effectively, the design-once-and-re-use-many-times model of digital IP now applies to analog IP for the first time. As the analog IP circuits in the Composa library have been extensively tested and used in previous designs, and are fully validated every time they are generated, this gives a similar level of reassurance to the digital IP world's 'silicon-proven'. All the major foundries are supported including TSMC, GlobalFoundries, Samsung Foundry and SMIC as well as other IC foundries and manufacturers.

About Agile Analog Ltd.
Analog IP needs to be different for each design. That is why Agile Analog™ has made a new way of doing things, conceived by some of the best minds in the industry. We provide a wide range of analog IP that is customised to your needs quickly, to a higher quality, and on any semiconductor process. Contact us at www.agileanalog.com to find out more.

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