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Review of Power Electronics Packaging and the Use of Copper Tungsten as Heat Sink

Power electronics is important in managing such applications as hybrid vehicles, power supplies, and induction heating to name a few. Power electronics mainly involves the control and conversion of an energy source from one form to another. The encasing of these devices requires design that will enhance thermal dissipation along with the improvement of electrical properties. The packaging of PE is termed as everything non-electrical that is required to convert an electronic circuit design into a manufactured assembly [1]. Packaging is one of the most important factors in efficiency of power electronics. With more sophisticated products being developed today, there are higher loads and stresses being put on the packaging of these semiconductor materials. Typical power electronics today include devices such as gate turn off thyristors, power MOSFETs, and insulated gate bipolar transistors (IGBTs) as seen below in figure 1.

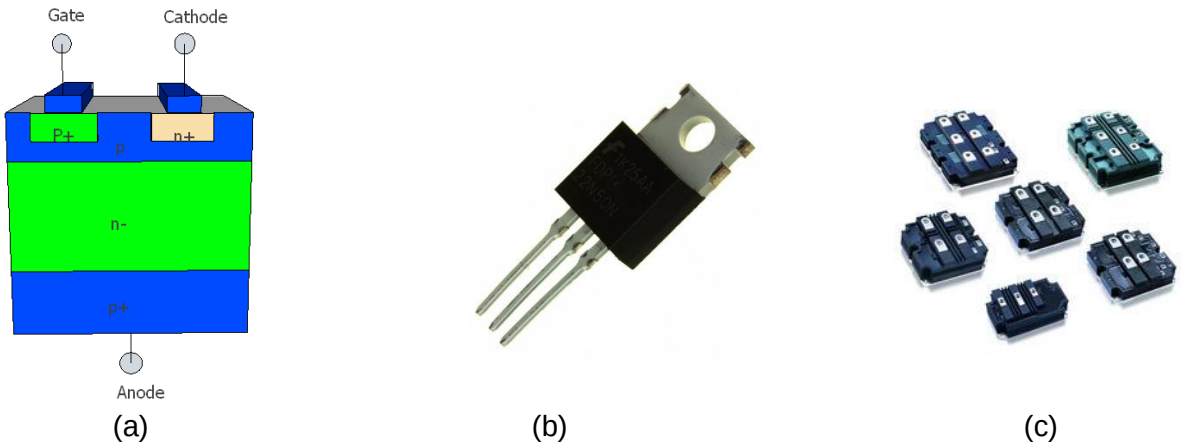

Figure 1. (a) Gate turn off thyristor representation with PN layers, turn on accomplished by positive current between gate and cathode (b) Power MOSFET (c) Insulated gate bipolar transistors

With an increase in demand and advancement of technology, there has been an equal need for advancement in the packaging of these devices. Semiconductor packaging provides properties such as mechanical support, electrical interconnection, heat dissipation path, and protection from the outside environment. Power electronics is used where there is

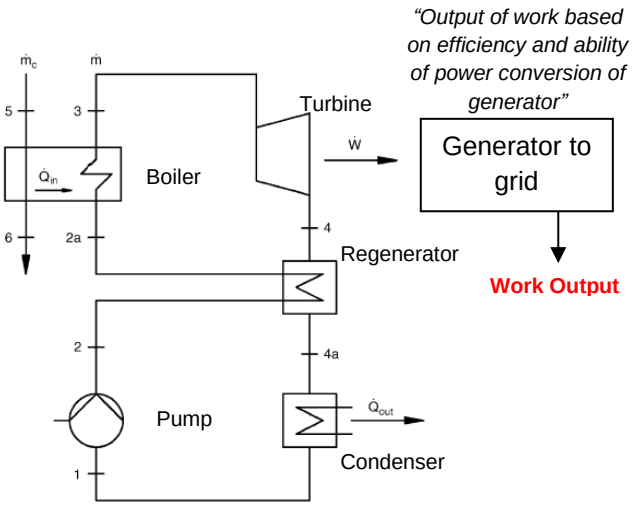

Figure 2. A more efficient power electronic package will create more efficient power conversions

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a need to alter a form of electrical energy. Higher currents and voltages in new systems mean higher thermal outputs and need of larger interconnections. Issues such as these spur the need for advancement in packaging technology. Namely thermal management, where problems such as mismatch of Coefficient of Thermal Expansion (CTE) in materials creates stresses and strains that would negatively affect the performance of the chip eventually leading to failure[2]. Three important factors pertaining to these devices are cost, reliability, and performance. Any small magnitude of loss is exponentially great for large systems. For example, in an energy generation system of a rankine steam cycle as seen in figure 2, every kW of power saved at the electrical generation (mechanical to electrical) end is much more valuable than energy saved at the thermal conversion end [3],. As mentioned by B.G. Fernandes, there are various losses in a cycle but with power electronics, more efficient power conversions can take place. The power electronics that is responsible for handling of electricity at the generator side is just as important as the mechanical and thermal processes that precede it. So with more efficient power conversions and storage there will be more saved in terms of cost and power consumption in the long term. To improve the characteristics of packaging, researchers have developed innovative methods for assembly.

3 dimensional packaging allows for lower resistance, higher current handling, and more effective integration [4]. Stacking of chips along the z axis can improve efficiency of power consumption and parasitic capacitance by up to 30%. Advantages of 3 dimensional packaging also include:

- Reduction in size and weight
- Increased quality of electrical signal due to reduced interconnection length
- Higher frequencies able to be reached
- Maximum use of available interconnects

Other methods for assembly include flip-chip process, pressure contact, thin film power overlay technology, metal posts interconnected parallel plate structure, and multilayer integration. These are novel concepts currently utilizing such materials as heat spreaders, DBC substrates, and 3 dimensional stacking.

How are Power Electronic Packages Assembled?

There has been an evolution in the methods of assembling from the wire bonding methods of the 1990's to the flip chip technology of today [5]. 2 dimensional packaging is quickly being replaced by 3 dimensional packages as these can be produced with enhanced characteristics while maintaining low costs. 3 dimensional structures are expected to bring higher power conversion density, lower parasitics, and enhanced system integration. This integration provides enhanced interconnection in devices such as power devices, driver circuitry, controls, sensors, and communication devices [5]. Methods such as wire bonding and 3D packaging are discussed below.

A) Chip on Board and Conventional wire bonding

Chip-on-board (COB) is a method of assembly where the microchip is directly mounted on and electrically connected to a circuit board. The method of COB can be described in three steps: 1) Die attach 2) Wire bonding 3) Encapsulation of die and wires [6]. Die attach is done by mounting a chip onto the board with a type of die adhesive. After this, a sintering process is done by heat so as to allow the adhesive to fully develop. Wire bonding is a type

of interconnection done in many applications of electronics by using gold or aluminum wiring as seen in figure 3b. Hundreds of these wire bonded interconnections are made within a module. The final step of encapsulation completes the process where an epoxy type liquid is used to coat the wires and the chip allowing for protection from the surroundings. This type of technology is increasing in size as more than 5000 LEDs are used in printer modules and state of the art multichip COB systems can carry over 100 chips on a single board as seen below [6].

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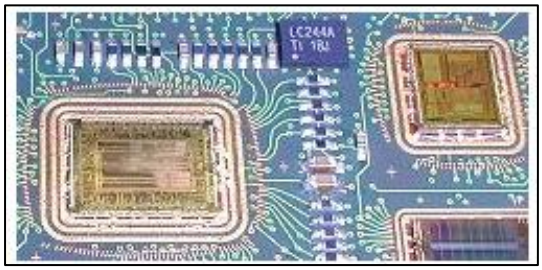
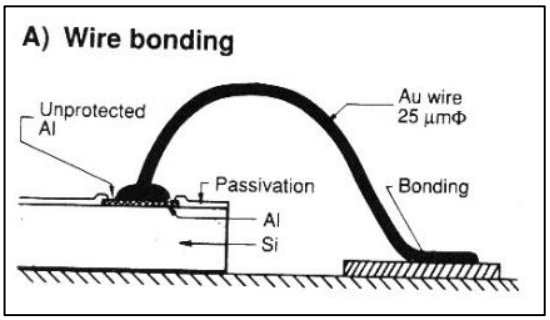


(a)



(b)

Figure 3. (a) Example of Chip on Board assembly [6]
(b) Bonding of frame to silicon chip via gold wire [7]

Compared to modern flip chip technology and 3 dimensional assemblies, chip on board and wire bonding are losing competitiveness. Wire bonding takes up large amounts of space inside a chip module. Characteristics such as speed and electrical quality suffer due to the extended lengths of interconnection used in bonding wires.

B) Flip-Chip Assembly

Electrical performance and size in flip chip technology is improved over conventional wire bonding and packaging. A chip with metalized bumps is placed face down on a substrate creating a direct electrical connection with the carrier [8]. A solder treatment with conductive epoxy and adhesive is done throughout the module and connections are made. The processing steps for the assembly are shown below.

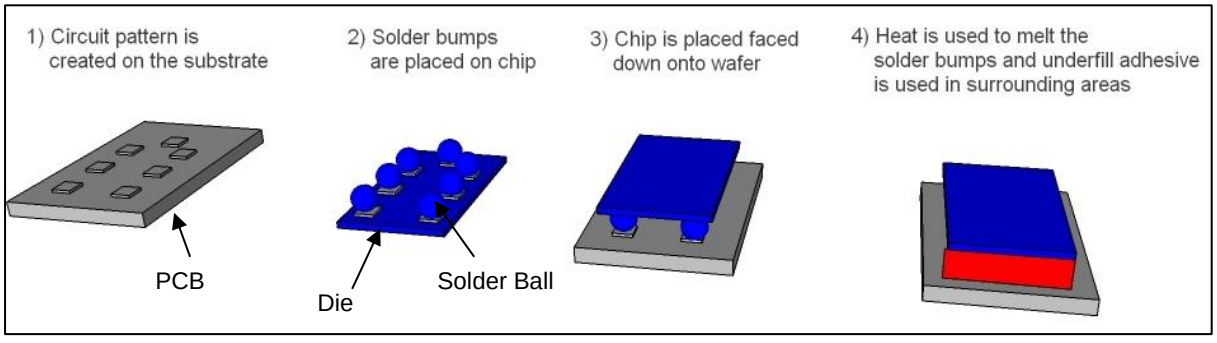


Figure 4. Flip Chip Process

The shorter length of bonding between the devices means decreased sizes with more quality connections being made. The inductance of the connection is reduced up to 10 times and the path is shortened from 25-100 times the length increasing speed [9]. A type of flip

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chip assembly with diagram and actual picture is shown below in figure 5. This arrangement favors thermal dissipation with a heat spreader mounted on bottom.

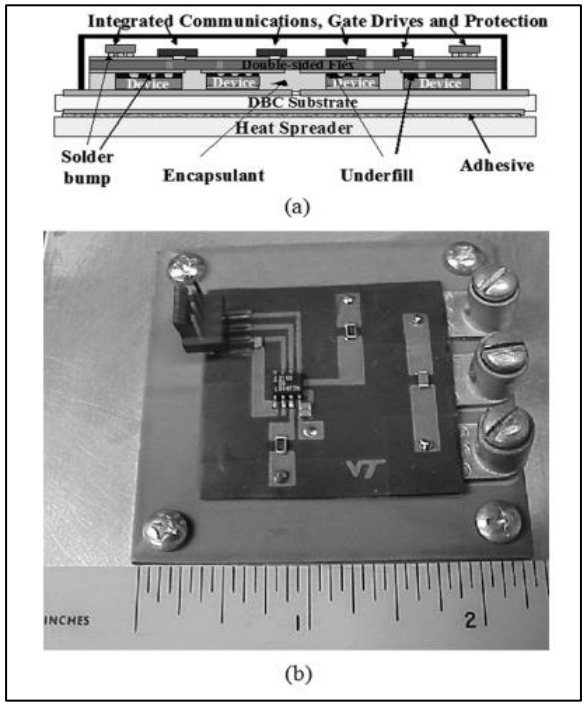

Figure 5. (a) Cross section diagram of flip chip flex integrated power electronics module (FCOF-IPEM) (b) Half bridge FCOF-IPEM [2]

C) Metal Posts Interconnected Parallel Plate Structure (MPIPPS)

MPIPPS is a 3 dimensional packaging technique used for power electronics that utilizes copper bonding rather than wire bonding. This method is a variation of the flip chip process. Copper “posts” are used to facilitate bonding which allows for lower DC resistance than conventional aluminum wire bonding [5]. This means less parasitic inefficiencies resulting in improved conversions of energy. The process for this assembly begins with achieving soldered contact by a metallization process that includes thin film deposition and electrolytic plating [5]. The next step in process is the attachment of copper posts by sintering in a gas controlled furnace. A top DBC is flipped upside down to be attached to the rest of the assembly creating a MPIPPS module as seen below. A heat spreader is also soldered onto the bottom. For thermal management the whole module is attached to a heat sink as seen in figure 5 b.

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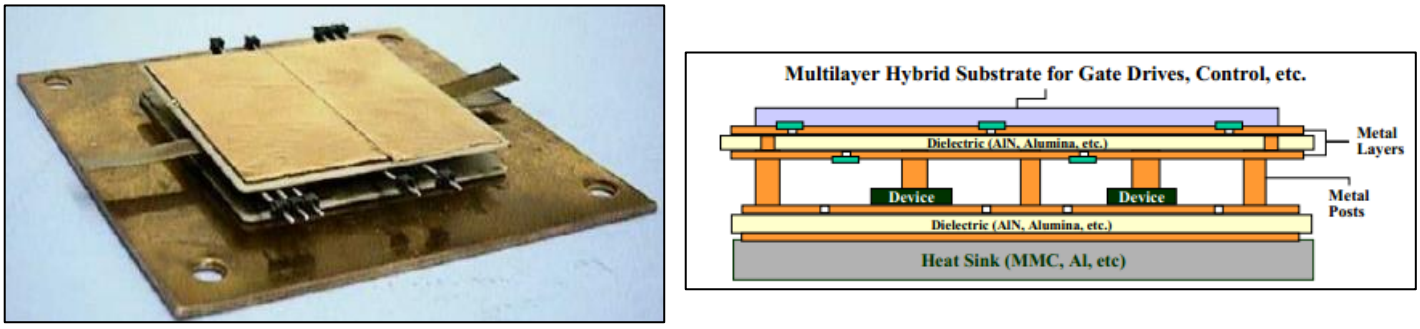

(a) (b)

Figure 5. (a) MPIPPS module (b) Diagram of MPIPPS device with copper posts [5]

This set up will allow more contact area for connections rather than wire bonding as can be seen in the comparison in figure 6. The larger contact area allows for large current handling and reduced electro migration [10]. Other advantages of MPIPPS include:

- Mechanical forces are distributed over a large area reducing stress
- Reduced parasitic inductance and capacitance
- Better heat dissipation paths due to metal posts
- Integration of passive components is possible through stacking between metal posts and metal layers

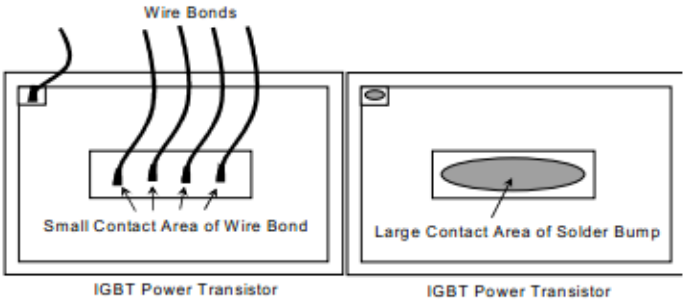

Figure 6. Wire bonding compared with solder bumping/posts

C) Pressure Contact Assembly

The pressure contact technique has been applied to high powered semiconductors such as diodes, thyristors, and GTOs [11] . The pressure contact method was designed to deal with the problems of wire lifting in wire bond techniques. Wire lifting occurs with thermal cycling and is not repairable. Pressure contact bypasses this problem by having a sandwich structure with anode and cathode sides in contact as seen in the figure below. This method does not require any soldering process and reduces residual stress on the components [5].

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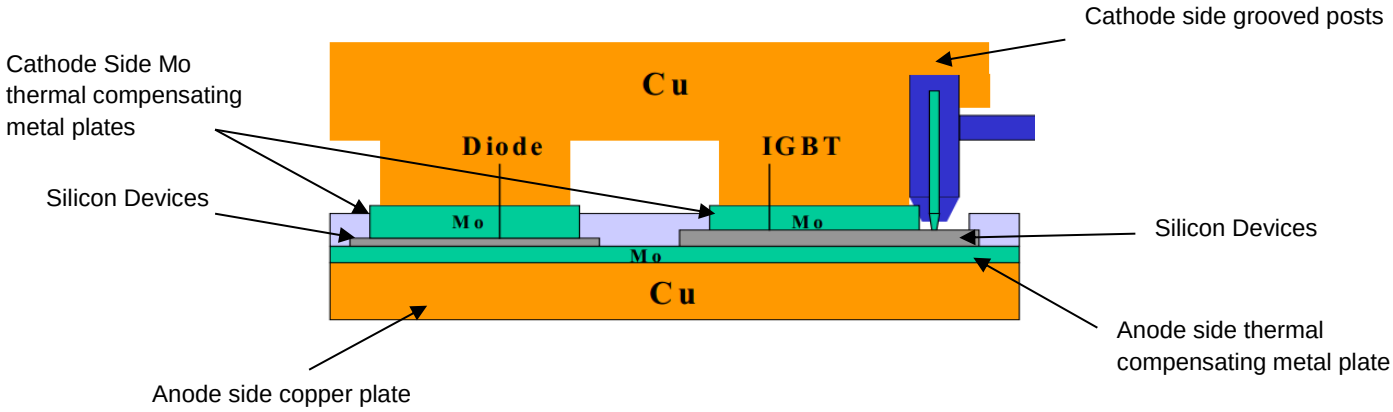

Figure 7. Diagram of pressure contact components in assembly [5].

Another method of pressure contact assembly uses a spring mechanism as the interconnection method. As presented by He et. Al., the process begins with a die mounting and soldering onto a substrate such as DBC. A gold plated copper pad is placed on top of the chip die for transition. The spring wire made of beryllium copper is soldered onto the plate as shown in the diagram below. On the top there is a PCB, emitter plate, and control/ICs placed in connection.

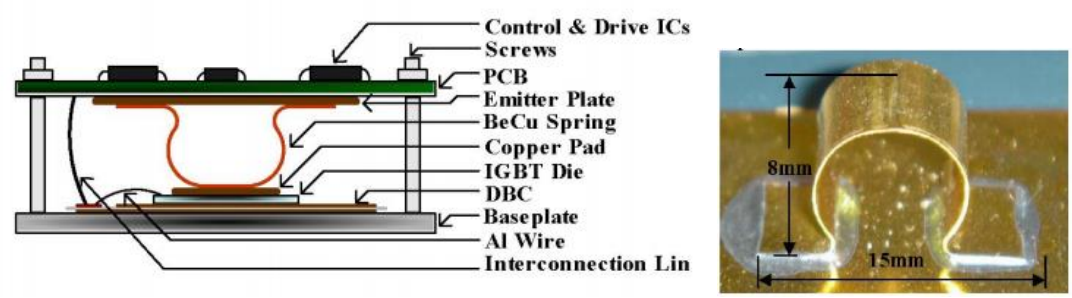

Figure 8. Pressure contact assembly [11]

Disadvantages of 3D packaging

Some disadvantages of 3D packaging include the need of high thermal dissipation due to such large power densities. As mentioned by Sarawi et. Al. methods of solution include:

- Distributing thermal energy across surface of 3D package
- Using low thermal resistance materials such as CVD (chemical vapor deposition) diamond
- Using forced air or liquid
- Using thermal vias (pathways) for dissipation

Other disadvantages include complexity, cost, and design software for these packages. Many of these problems are being addressed with further advancement in manufacturing technologies.

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Electrical and Physical Parameters of Packaging

The dimensions of a package are important in the properties of the overall package. With 3 dimensional packaging, less wire bonding length is needed and reduction in size can be achieved. The decreased size results in maximum use of raw materials. Thermal efficiency is important for creating a well functioning reliable package. Problems like delamination occur at the meeting junction of bonds with thermal cycling. Finite element thermal analysis is shown in figure 6 of both wire bonding and MPIPPS. Failure can occur at the solder joints where interconnection bonding takes place. Heat sinks and thermal spreaders assist in thermal cycling so debonding does not occur.

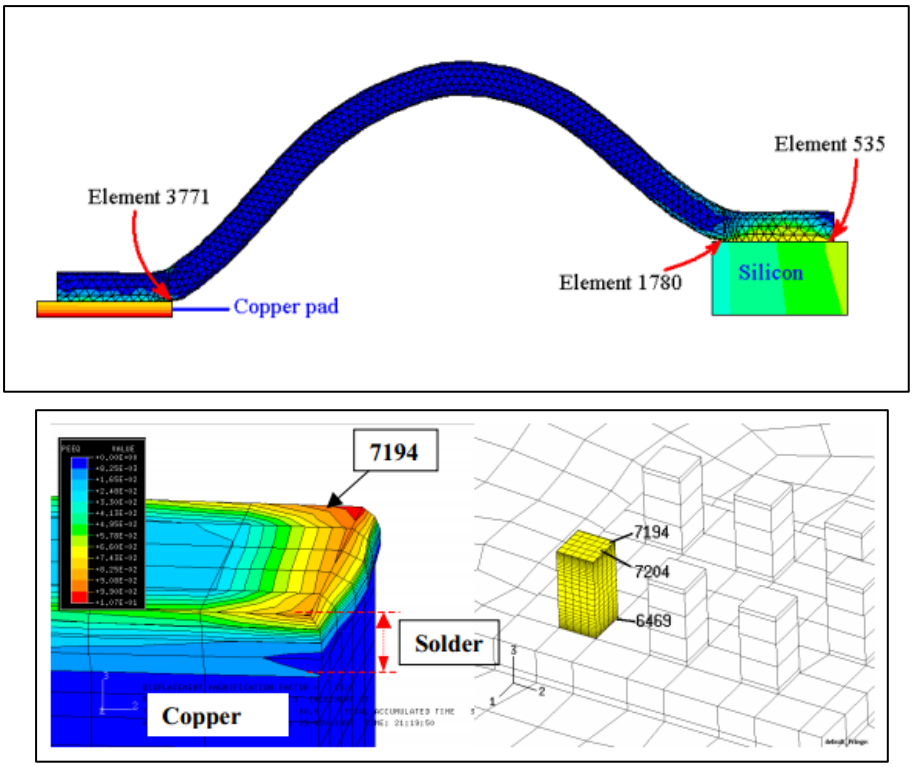

Figure 6. Finite element software analysis of wire bonding and MPIPPS structures [5].

Delay is another electrical parameter used to refer to the time it takes for a signal to travel between points in a system module. Time is proportional to interconnect length [review of 3D technology [12]. With interconnection lengths being reduced, delay is also reduced. Length is an important part of an electrical parameter called noise. Noise is the unwanted disturbances that inhibit quality signal transfer. Reflection, crosstalk, simultaneous switching, electromagnetic interference are all noises that need to be reduced in magnitude for improved performance. Power consumption is also a major factor that is described in equation below.

$E = CV^2$, energy dissipated in electronic system

$P = fCV^2$, power consumption

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Where, $E = energy\ dissipated$
$C = interconnect\ parasitic\ capacitance$
$P = power\ consumption$
$f = number\ of\ transitions$
$V = voltage\ swing\ across\ C\ and\ f$

The power consumption formula describes how power consumption is in direct correlation with parasitic capacitance. Packaging techniques such as flip chip or pressure contact reduce these parasitic therefore reducing the power consumption. The speed, f, is also increased by the same relationship. In analysis done by Reinhold [4], multichip 3 dimensional modules would consume 2% power as opposed to printed wire boards which would consume up to 10%. This means a reduction on thermal stresses and an associated longer lifetime.

Integration of Copper Tungsten (CuW) as Heat Sinks for Packaging Electronics

Warping and thermal stresses is one of the primary factors in designing packages. Power semiconductors, optoelectronics, and high power RFs are just some devices that need thermal stressing to be taken into account. High temperatures are such an issue that even liquid cooling has begun to be discussed as options. This method would present problems of cost and new industry development so it is best to work with materials currently being mass produced. Thermal stress occurs because of the difference in the coefficient of thermal expansion (CTE) of the materials that are bonded together. Because of this factor, materials such as the die or substrate can expand at a different rate than the device causing delamination as discussed before. The CTE of the solder being used must be taken into account also, since this will be the point of contact between the two materials being bonded. The CTE of usual semiconductors and ceramics ranges from 2-7 $\frac{ppm}{K}$ [13]. As seen in the table below of heat sink materials, the CTE of tungsten fiber reinforce copper (CuW) ranges from 5.7-8.3 $\frac{ppm}{K}$.

Reinforcement	Matrix	Thermal Conductivity k (W/m-K)	CTE (ppm/K)	Density (g/cm³)	Specific Thermal Conductivity (W/m-K)
—	Aluminum	218	23	2.7	81
—	Copper	400	17	8.9	45
—	Invar	11	1.3	8.1	1.4
—	Kovar	17	5.9	8.3	2.0
—	Cu/I/Cu	164	8.4	8.4	20
—	Cu/Mo/Cu	182	6.0	9.9	18
—	Cu/Mo-Cu/Cu	245 to 280	6 to 10	9.4	26 to 30
—	Titanium	7.2	9.5	4.4	1.6
Copper	Tungsten	157 to 190	5.7 to 8.3	15 to 17	9 to 13
Copper	Molybdenum	184 to 197	7.0 to 7.1	9.9 to 10.0	18 to 20
—	Solder – Sn63/Pb37	50	25	8.4	6.0
—	Epoxy	1.7	54	1.2	1.4
E-glass Fibers	Epoxy	0.16 to 0.26	11 to 20	2.1	0.1

Table 1. Thermodynamic properties of various thermal management materials [WEBPAGE]

The range of 5.7-7 $\frac{ppm}{K}$ matches comparatively well with the semiconductor and ceramic material. Although bare copper by itself has much higher thermal conductivity, the CTE is

much too high to be matched well in an assembly. Copper's expansion rate would cause failure after only a few cycles. On the other hand, copper tungsten is well suited for reliability and long life time cycling. CuW consists of an alloy between 10 to 50 weight percent copper and the remaining is tungsten [14]. The tungsten role in this alloy is to lower the expansion rate of copper. In commercial products, CuW is suitable for heat sink applications that provide effective thermal management and cost effectiveness compared with other materials. With increasing electrical energy production comes higher thermal output. An increase of tungsten content can lower thermal expansion rate conserving the quality of signal in power electronic modules.

Heat sink design requires considerations in the material used in bonding as proposed by Aeroflex, a company specializing in microelectronic equipment. Some key factors to consider in mounting chip devices are:

- Flatness of mating surfaces to maximize bonding area
- Use of thermal compound to fill any microscopic voids
- Stress relief tab (as seen in figure 7a), helps with reducing mechanical stress on joints

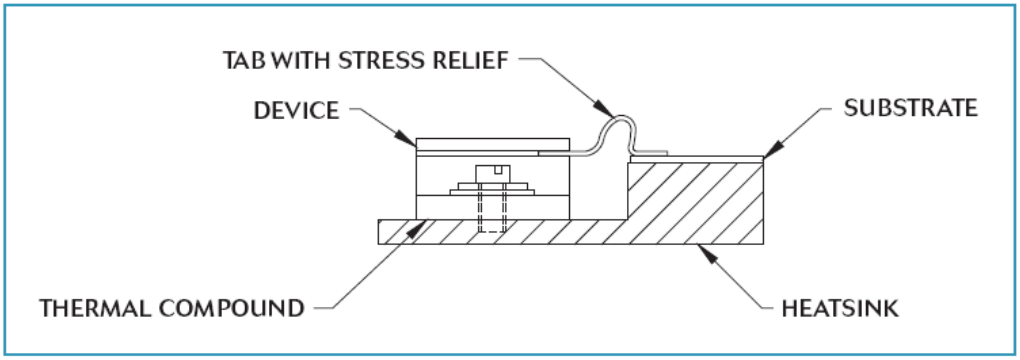

Figure 7. Aeroflex Mounting Application [15]

Solder joint compounds are crucial for lifetime design purposes. An increase in temperature can mean accelerated degradation of solder joint properties. The solder-SN63/Pb37 has a high CTE of 25 $\frac{ppm}{K}$ with a low thermal conductivity of 50$\frac{W}{m-K}$. The effects of steady state temperature and thermal cycling need to be observed in the design process as well as the thickness of the solder. Muralidharan [16] has done experiments on types of solder when joining between AlN DBC with Cu/Ni (P)/Au (fig8). The type of solder used is lead free Sn-3.5Ag. The thermal cycling process was done between 5˚C and 200˚C holding for 30 minutes at 200˚C and for 5 minutes at 5˚C. This test was for a module that would reach high temperatures up to 200˚C encountered in hybrid and electric vehicles. The result showed reductions in thermal diffusivity occurred and significant damage was seen after 3000 cycles. The type of solder used in bonding is important for heat sink and power electronic connections.

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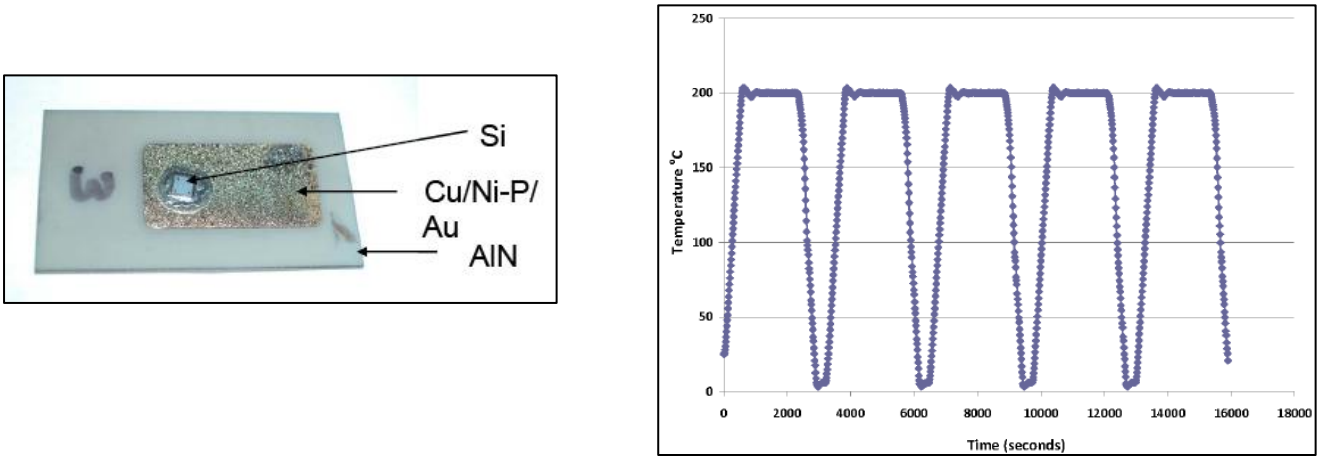

(a) (b)

Figure 8. (a) Chip module assembly arrangement. (b) Thermal heat cycling method. Minimum temperature of 5˚C and maximum temperature of 200˚C applied. [16]

Conclusion:

Advancement in power electronic packaging is necessary as higher power densities are achieved and thermal output is increased. Packaging is crucial in applications such as renewable energy. Optimal performance of power electronics packages is essential for harvesting renewable energy such as solar power, wind power, and fuel cells. This can be true also for utilization of fossil fuels. The energy that is available must be preserved and not loss due to inefficiencies. Thermal dissipation is one of the key parameters in development of packaging. For example, Temperatures as high as 150˚C can be seen in new 1200 V-IGBT4 modules [17]. 3 dimensional packaging techniques offer better thermal management, smaller size, lower resistance, and higher reliability. Power devices differ from other electronics in that they tend to handle large power currents and therefore require thick interconnections as well as better thermal management. CuW has the necessary properties to be applied as heat sinks for power electronic packages. The coefficient of thermal expansion (CTE) is relatively low compared with other materials in the same class. This means cracking and failure due to expansion and contraction is no longer a problem. At the same time thermal conductivity is of high rating and is able to dissipate heat efficiently. With proper packaging of electronics, greater generation and transmission of available energy sources is possible.

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