Packaging Fault Isolation Using Lock-in Thermography

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Addressing the challenges of modern package failure analysis

Performing accurate package failure analysis has become a greater challenge than ever before, due to the increasing complexity of packaging and module technology. Board space reductions and tighter integration have led to smaller pitches and increased complexity at interconnect levels in interposers and substrates.

In order to address this increasingly complex and challenging package environment, FA groups need to take a new approach that allows them to simply and effectively identify the source of package failures. This is where lock-in thermography (LIT) can help.

Lock-in thermography and the ELITE system

Lock-in thermography (LIT) is a failure analysis technique that has unique applications to package-related failures. Compared to other failure isolation techniques such as liquid crystal imaging, LIT provides better spatial resolution and 3D analysis capabilities. [1-3] LIT is a logical choice for the "first stop" in the analysis process.

LIT functions by observing temperature increases in a package, in the form of thermal emission at the package surface. LIT generates easily interpreted hotspot images, making it a powerful, high-resolution tool for failure site isolation. [4]

The ELITE (Enhanced Lock-In Thermal Emission) system from DCG Systems provides a full range of LIT capabilities, in addition to support for computer automated design (CAD) navigation and alignment to make determination of failure locations more accurate.

Existing package failure isolation techniques

Today, most package failure analysis is performed using "grind and find" techniques. These techniques are typically tedious and risk destroying evidence of the fault, unlike LIT.

Other techniques, such as time domain reflectometry (TDR) and magnetic imaging, lack some of the benefits offered by LIT, but can still be useful in certain situations. For instance, TDR is particularly effective at determining the location of opens in

interconnects that are connected to an external pin. By measuring the time required for an electrical pulse to be reflected at a high resistance or open, the distance into the package can be accurately determined. Unfortunately, this technique cannot be readily applied to interconnections between chips, nor to short-circuit faults.

Magnetic imaging [1] relies upon the variation of magnetic field with distance between current path and detector. When the current can be restricted to the failure path, magnetic imaging can be useful for tracing pin-to-pin leakages. However, when multiple current paths are involved, the complexity of analysis rises and accuracy declines, particularly when these paths are close together.

Reducing noise with LIT

Phase-lock methods are used for many types of measurements, providing significant improvement in sensitivity over traditional detection techniques by reducing noise. In LIT, an electrical stimulus causes heating at the failure site, which is detected when it reaches the surface being inspected. The thermal emissions are measured using a free-running infrared camera. By observing the signal in phase with the electrical stimulus, noise can effectively be averaged out, because background thermal signals associated with emissivity and static bias heating are out of phase with the stimulus signal (see Figure 1).

Fault depth determination

There is a delay between the electrical stimulus and detection of the failure-related signal, because the heat generated by the failure takes time to reach the surface of the package. If we understand the thermal conduction properties of the device, the depth of the failure can be calculated from the delay.

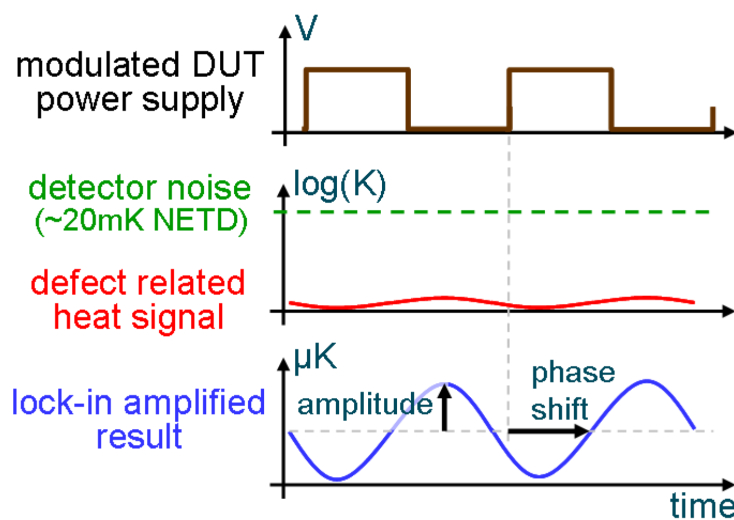


Figure 1: Lock-in techniques can reduce the impact of noise and enhance detection of smaller signals.

By performing the lock-in measurement on a pixel-by-pixel basis (see Figure 2), a map of localized heating can be created to indicate the lateral position of the failure, while the phase delay at that pixel indicates the depth of the failure.

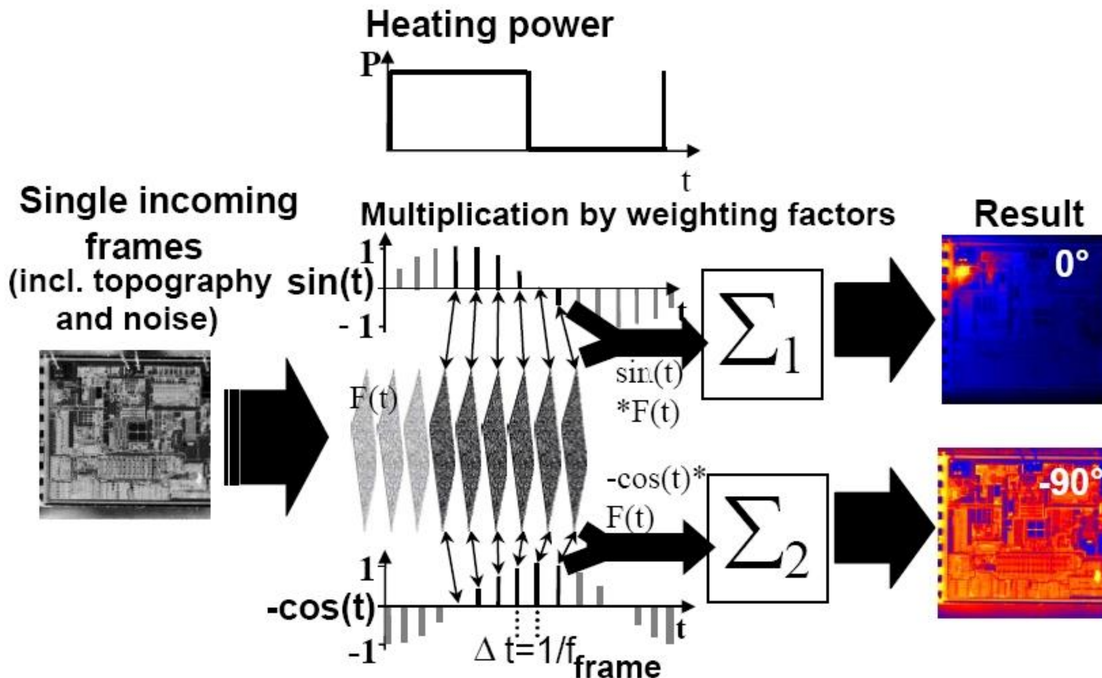


Figure 2: Lock-in thermography can provide a pixel-by-pixel analysis of a heat signature caused by a short circuit.

Experimental setup

In the examples cited below, a DCG Systems ELITE lock-in thermography system was used. The ELITE system has the ability to accept a wide range of electrical stimuli and includes an infrared detector, proprietary infrared objectives, a solid immersion lens (SIL) for high magnification if required, CAD overlay for navigation and precise failure localization, and a data analysis package.

Wire-bonding failure localization with ELITE

In this example [2], electrical analysis indicated a bond-wire short with a resistance of ~1Ω. TDR indicated a failure site different from the site that was eventually found. Multiple X-ray analysis efforts also failed to accurately locate the failure site.

Low-resistance shorts have historically been very difficult to isolate using thermal techniques, because such shorts dissipate very little heat. In this case, about 10mW of heat dissipation was generated at 100mV lock-in voltage, yet ELITE localized the fault in less than 1 minute.

The initial localization is shown in Figure 3. Phase-shift analysis was used to determine the depth of the fault in the package. The fault depth (600 μm) correlated with the bond-wire routing in the package, also shown in Figure 3.

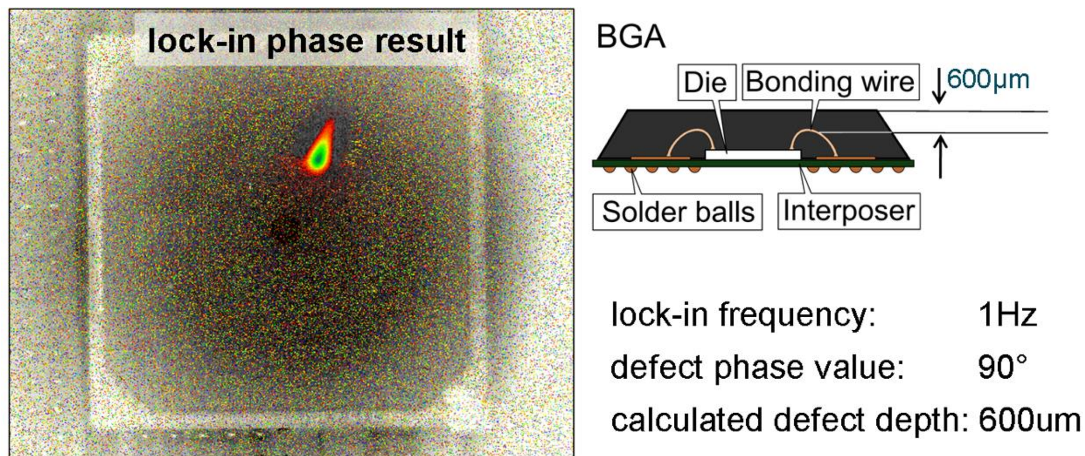


Figure 3: Localization of a bonding wire short using lock-in thermography.

Based on the location provided by lock-in thermography, the engineer was able to use high resolution X-ray imaging to quickly identify the cause of the failure, as shown in Figure 4. X-ray alone would not have been able to isolate the defect within a practical measurement time.

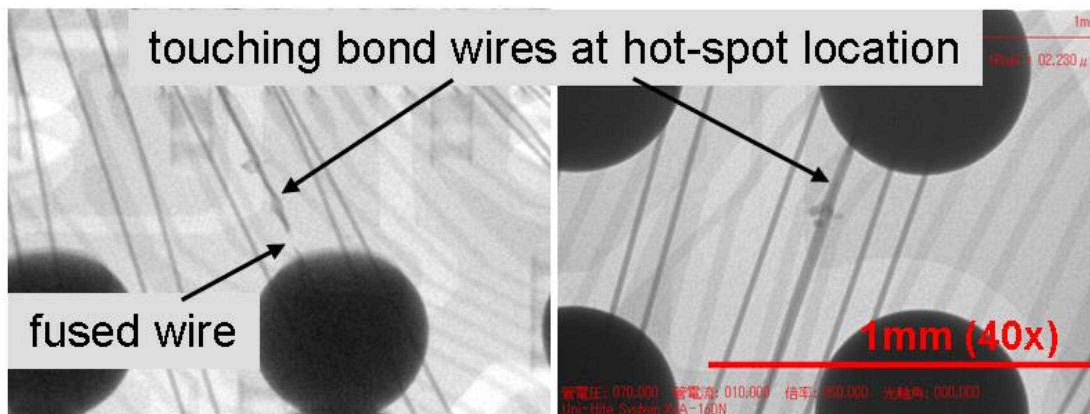


Figure 4: High-resolution 3D X-ray images of the defect location found using LIT.

LIT for small packages

Smaller packages can have printed circuit board (PCB) substrates rather than traditional lead frames. Since these substrates have multiple interconnect levels where faults can be hidden, they add another level of complexity to the package failure analysis process.

An internal PCB-based device, shown in Figure 5, had a 2Ω short from Pin 2 to Pin 3. ELITE successfully isolated the short to a tin filament, shown in Figure 6.

Since decapsulation can destroy evidence of the short, it is critical to understand the precise location of a short before attempting decapsulation or delayering. Identifying root cause using cross-section analysis is also more successful when the location of the short is well known beforehand.

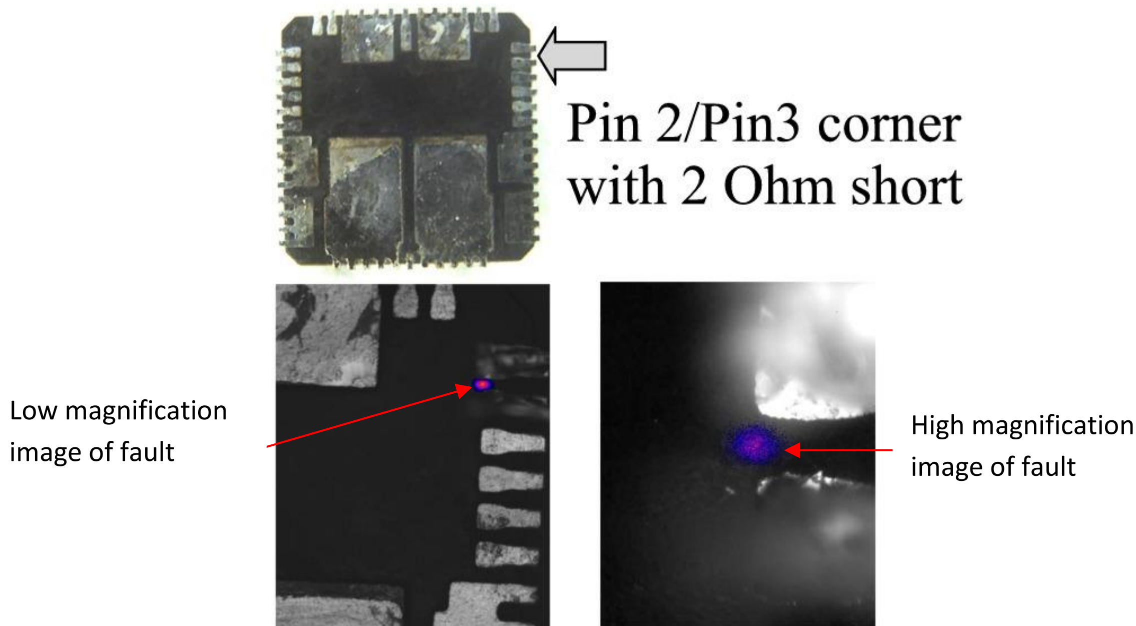


Figure 5: Image of package and LIT results. Top left image is optical image of entire part and lower images show higher magnification images with thermal fault overlaid.

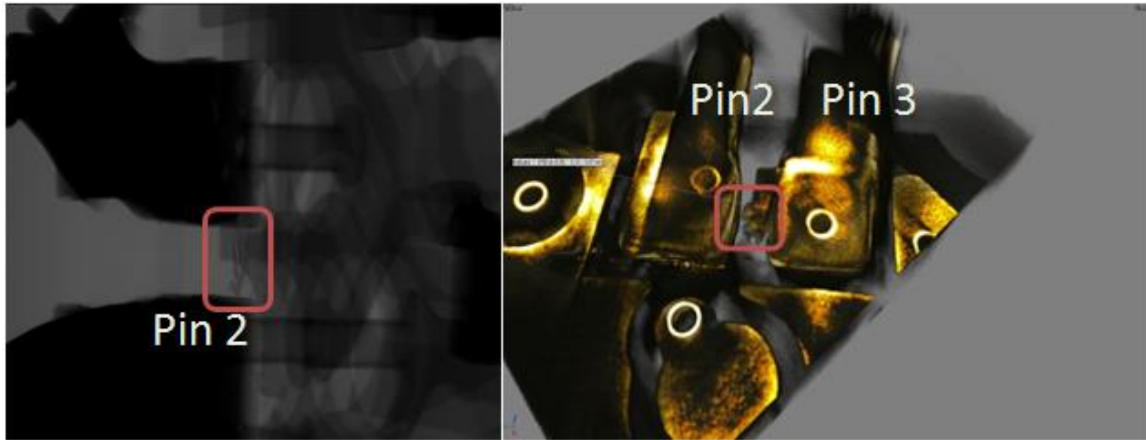


Figure 6: 2D X-ray and 3D X-ray tomography images showing the tin filament that was found to cause the electrical short.

LIT for redistribution layer failure isolation

Redistribution layer (RDL) plating is added to the top of a finished die to allow denser connections to the completed chip. It is also useful for resistance reduction for interconnects, as in the case below.

This case study illustrates how LIT can isolate a failure at a leakage level that would be below the sensitivity limit of techniques like optical beam induced resistance change OBIRCH and liquid crystal imaging. The 5Ω short in the redistribution plating was successfully isolated to a small area by the ELITE system, as shown in Figure 7. The device was partially decapsulated to expose the redistribution layers and cross sectioned to find the defect: a copper filament (see Figure 8). Without first determining the precise location of the filament, cross-section analysis would have been unsuccessful.

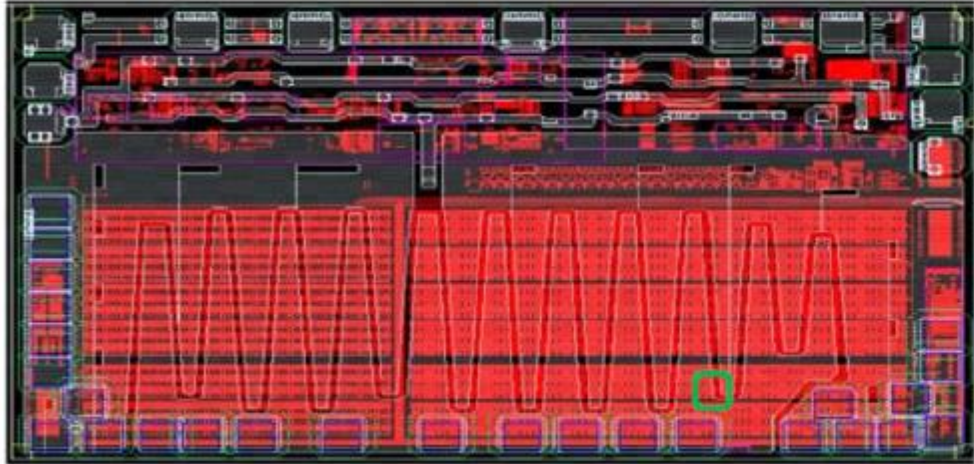
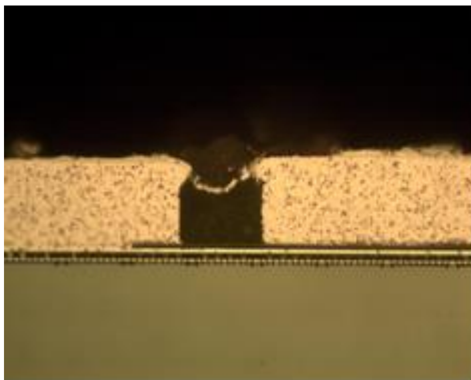


Figure 7: The green box indicates the isolated area for the short in the RDL level.



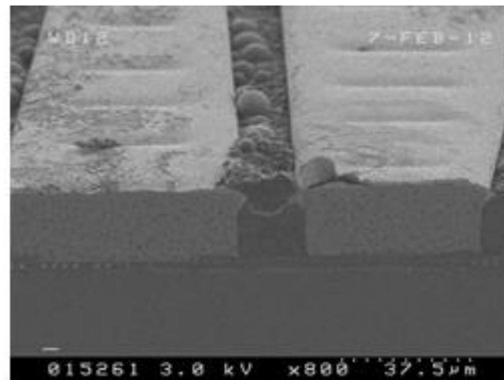


Figure 8: Optical and scanning electron microscopy (SEM) images of the cross section of the failed area identified by the ELITE system, showing a copper filament.

LIT for stacked die

The 3D fault localization capability of the ELITE system was illustrated by using an FIB (focused ion beam) to create a thermally active defect at the substrate level. [3] Die were sequentially stacked on the defect (see Figure 9) and the phase delays in the LIT signal were measured as a function of lock-in frequency (see Figure 10) as each die was added.

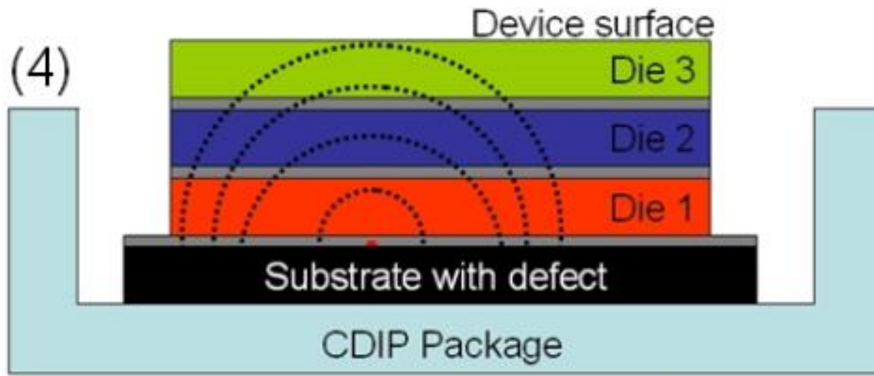


Figure 9: A defect in the substrate was generated with an FIB before stacking.

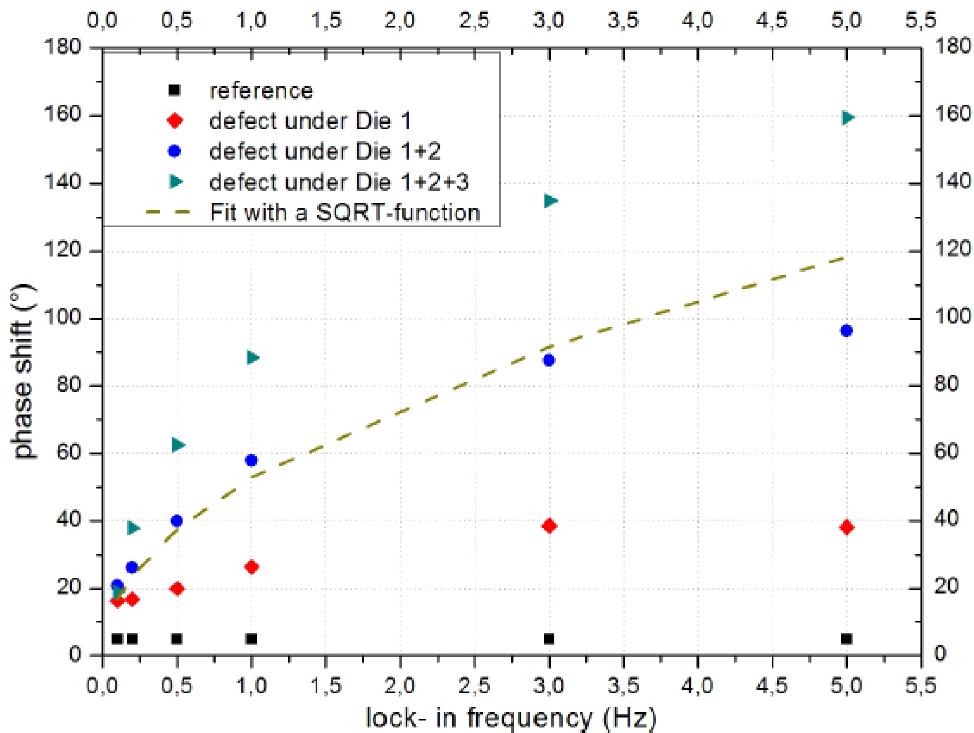


Figure 10: Phase shift versus lock-in frequency for example shown in Figure 9, with three die stacked on a substrate containing a thermally active defect. The theoretical curve for the two-die stack, based on knowledge of the thermal properties and thicknesses of both die, shows good agreement with experimental data.

Figure 10 clearly shows that the depth of a thermal defect can be determined, given knowledge of the thermal conductivity of the materials and thicknesses of each layer.

LIT applications for advanced interconnections

Interconnections within a package have drastically changed with the rapid rise of multi-chip packages. Through-silicon vias (TSVs) are one of the common advanced interconnect structures, and the ELITE system can localize the depth of TSV failures to ±20 µm.

In the case illustrated below, [6] electrical measurements indicated a fault between the copper TSV and silicon substrate, with a diode characteristic. Standard backside LIT localized the fault. Figure 11 shows the defect observed at the predicted location on the TSV: a hole in the glass liner between the TSV and substrate.

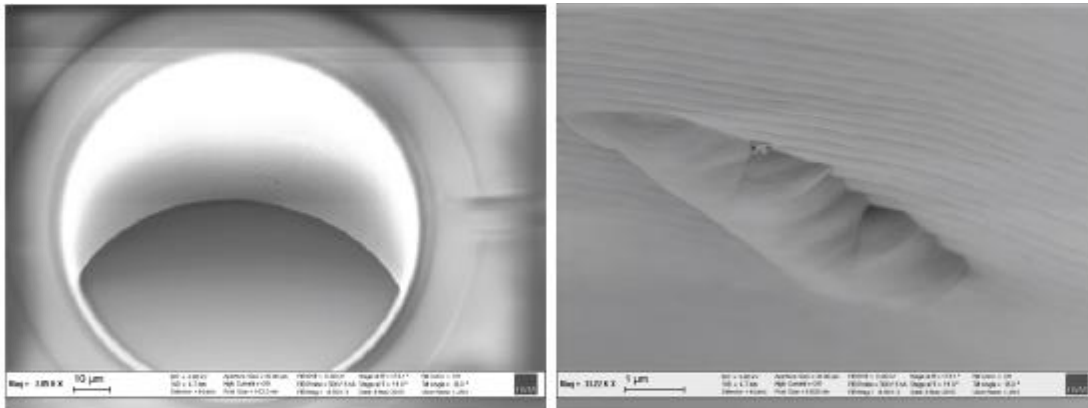


Figure 11: SEM images of the defective TSV (left) and the TSV sidewall defect (right) after deprocessing.

Conclusion

The increased complexity of microelectronics packaging has made lock-in thermography a critical part of the failure isolation toolkit. The examples provided in this article have shown that lock-in thermography is an effective tool for 3D isolation of electrical faults in both small and large packages, within wire-bonding, chip-scale packaging, redistribution lines, stacked die and advanced intra-chip interconnections.

Previous work has established the value of LIT for high-resolution electrical fault isolation in the die [4], and for PCB failure isolation. [7]

DCG's ELITE system supports initial determination of whether a failure is package-related or die-related. It also supports further isolation of the failure at both the package and die level.

References

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