Recent Advances in Die Attach Film

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Abstract: The advantage of using die attach film at the wafer level compared to using die attach material on individual die are known for many years. To completely take advantage of the use of die attach film at the wafer level, the die attach film has to be optimized to account for various process conditions that the film has to successfully pass through without degradation in any of its end use properties of adhesion strength and thermal and electrical properties.

More recently, the demand for hand held devices has led to more advanced technologies in 2.5D and 3D packaging and in the handling of extremely thin wafers and dies. The material supply industry has responded in providing newer generations of die attach films and wafer protection material to these increasingly demanding challenges.

In this paper, we will examine the criteria for higher efficiency, more reliability and higher performance die-attach film at the wafer level.

We will also examine the effects of interconnection from chip to package on the choice of die-attach solutions. The packaging using wire-bonding, flip-chip soldering or the direct mechanical contact attach from flip-chip to bond pads effectively dictates the choice of different wafer level die-attach solutions.

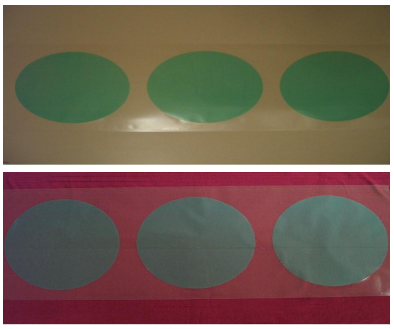
Interconnections in Wafer Level Die-Attach and Packaging:

In high volume commercial applications, the use of 10-20 micron die-attach film adhesive has been proven to be reliable for stack-chip from 2-3 layers. The 10-20 micron film adhesive not only yields thinner devices that are attractive for tablets, cell phones, and cameras, it also provides more uniform and controlled flow of the adhesive and thus more reproducible interconnections.

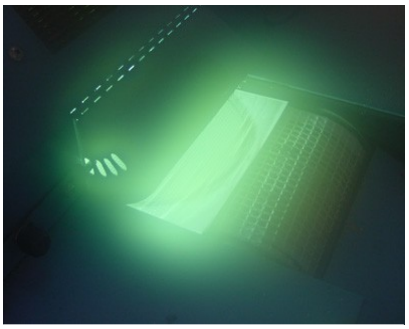
The standard wire-bonding chip packaging uses backside die-attach that can use more traditional epoxy die-attached film adhesives that are available from die-attach film adhesive manufacturers from US[1] and Japan. Figure 3 below is a pre-laminated wafer with 15-micron thin die-attach film adhesive.

Typical manufacturing process in using wafer level packaging are now integrated in terms of using dicing tape and die-attach film that are directly laminated on the wafer before dicing. The layer of such configuration can be represented in Figure 1 below:

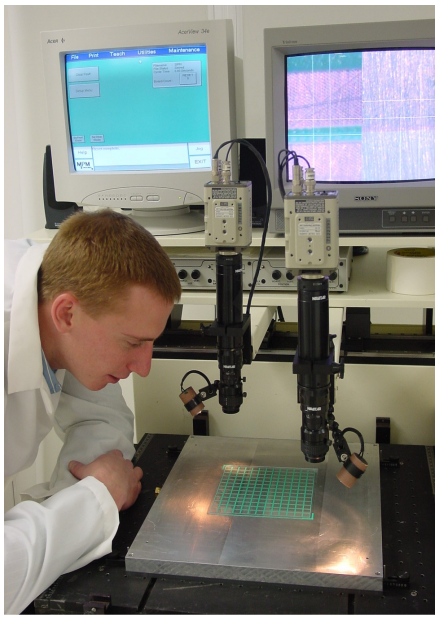
[1] AI Technology, Inc. http://www.aitechnology.com/products/dieattach/



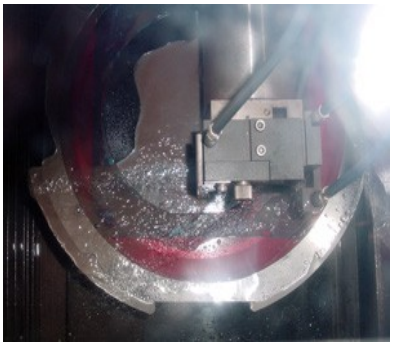
Lamination of wafer onto dicing die-attach film (DDAF)



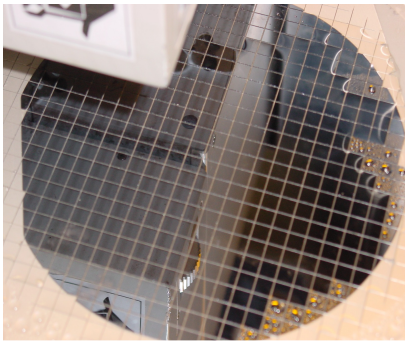
Shining UV to release dies



Examining dies for packaging



Dicing wafer with DDAF



Pickup dies from DDAF

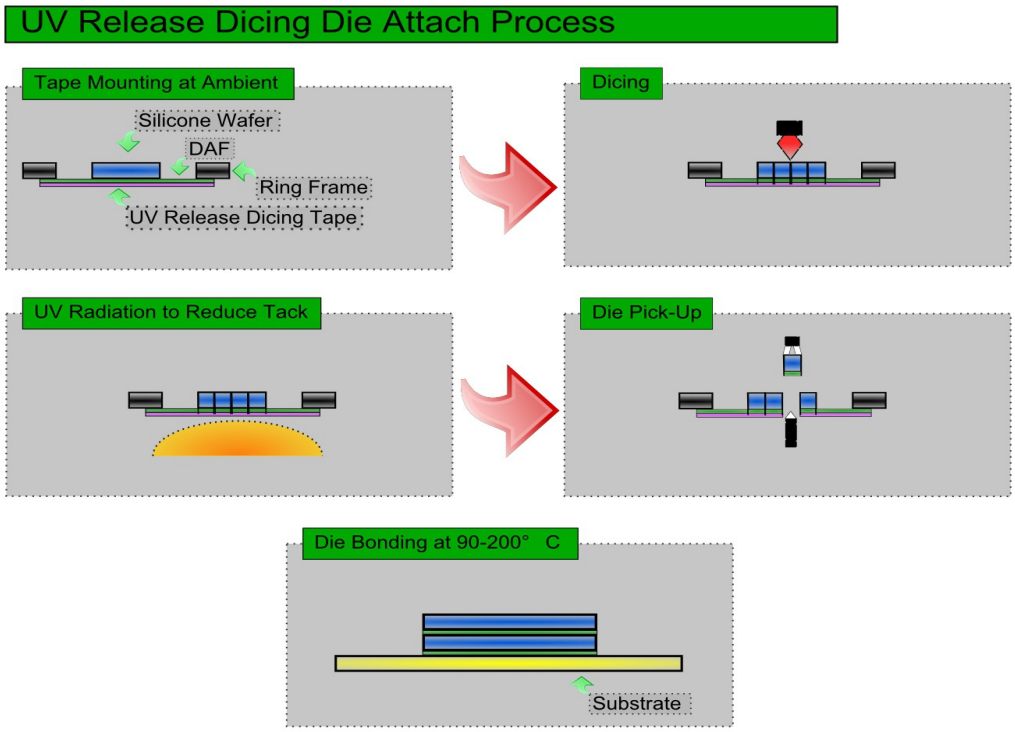


Figure 1: Dicing Die Attach Film Processing: Die Attach Film must be compatible with UV release layer and have the ability to flow and cure rapidly or flow with light pressure and cure without pressure to maintain productivity.

Relationship between Die-Attach Adhesive Properties and Device Performances:

The material technology challenges that allow for the processes described in Figure 1 are many and have been met so far by dicing die-attach film (DDAF) adhesives from US and Japan. These challenges include:

1. Very thin and stable film adhesive (typically epoxy-based) of 10-25 micron.
2. DAF film adhesive must be compatible with the adhesive layer of the dicing tape to prevent cross-contamination leading to residues and other side effects.
3. Ability to allow chip-stack bonding with high efficiency.
4. Ability to provide die-bonding stability for wire-bonding operation of up to 250°C for the highest production rate possible.
5. Most of the existing DDAF are meeting the performance requirements of at least JEDEC IPC level 3 or better for moisture sensitivity after packaging.
   - Depending on the bonding stability and moisture sensitive properties of DAF and the molding, encapsulation or other electro-mechanical protection, the finished devices range from level 3 in most cases and for the best solution meeting the level 1 requirement.
   - In case of high temperature applications beyond typical 125-150°C, newer non-epoxy DAF can now withstand long-term usage of 200°C and beyond.

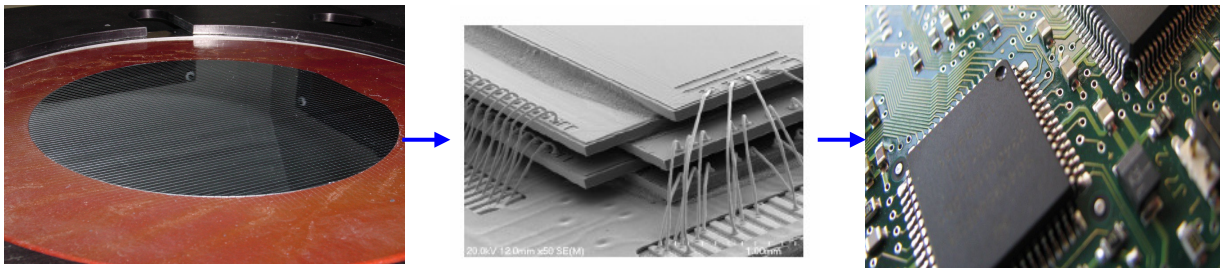


Figure 2: Semi-conductor packaging from wafer DDAF to component on board: different DAF moisture sensitivity, devices may reach level 1 to 3 moisture sensitivity even with the best of electromechanical encapsulation and protection.

New Generation of Semi-Conductor Packaging Requires Advanced Die Bonding Adhesive and Stress Relief Protection:

Traditional flip chip uses wire-bonding and solder-bump reflow for most requirements. The higher speed, performance and cost continue to drive the semiconductor packaging toward shorter path of interconnections between each level of the stack-chip packages.

The need to lower the cost of packaging has led to many innovative packaging solutions. The lowest cost electronic devices such as UHF RFID tags have been produced using direct flip-chip mechanical compression contact successfully in large volume.[2] However, they are limited to operation temperature of less than 60°C and they are not very stable against moisture.

[2] Alien Technology and RFID: Roll-to-roll processing of silicon-based microelectronics http://usms.nist.gov/workshops/macroelectronics/05-Alien.pdf

The fact that contact resistance can be properly maintained for long-term usage within specified temperature and environmental constraints provide hope that solutions for high performance applications can be achieved with more engineered materials and packaging.

Figure 3 below is the illustration of such flip chip direct contact interconnection:

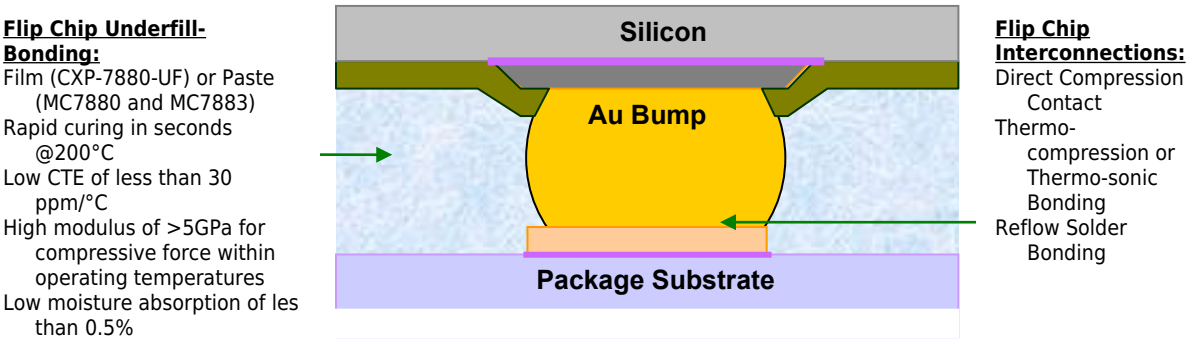


Figure 3: Flip chip interconnection with direct mechanical contacts between precious metal bumps and preservations on chip and package substrate respectively.

The key for performance for this type of package is the flip-chip underfill that must also perform as a stable die bonding adhesive. For the flip chip underfill-adhesive to function properly, they must possess at least the following characteristics:

1. Underfill-adhesive must be easily placed either on the substrate or on the interconnection front side of the chip. Dicing die-attach film (DDAF) will still be applicable. If paste underfill-adhesive is to be useful, it must stay in place after dispensing onto the substrate or chip.
2. The underfill-adhesive must not prevent contact when the chip and package substrate interconnections are lined and compressed for bonding. Unlike the use of Z-axis, uni-axial, conductive adhesive, any particulate could be detrimental for the achievement of interconnections.
3. High glass transition temperature and modulus to maintain the electrical contact and characteristics. For commercial and military applications, it should be well above 150°C.
4. The underfill-adhesive should be as low in coefficient of thermal expansion (CTE) as that of higher filled traditional epoxy underfills (< 30 ppm/°C).
5. In order to provide reasonable productivity, the underfill-adhesive must be capable of curing at 175-250°C in less than 10 seconds.
6. To meet the JEDEC/ IPC Level 1 moisture sensitivity requirements, the moisture absorption should be well below 0.5% in saturation.

There are now non-epoxy based, high temperature, underfill-adhesives in paste or film format in thickness of 25-75 micron for such applications.

Through Silicon Via (TSV)[3] Interconnection Requiring Specialty Underfill and Via filling for Stress Relief

Through Silicon Via (TSV) stack chip packaging represents the ultimate chip interconnection performance for stack chip packages. The requirement for stress relief is even more critical to filling in the vias of the TSV structure and between the stacking chips.

For filling in the TSV vias, the specialty fill-in-adhesive requires at the following characteristics:

1. The fill-in-adhesive must have extreme low viscosity to wick into the vias easily with the capillary forces.
2. Once cured, they must have very low coefficient of expansion (CTE) and preferably substantially below 30 ppm/°C.
3. High glass transition temperature and modulus to maintain the electrical contact and characteristics. For commercial and military applications, it should be well above 150°C.
4. Again, fill-in-adhesive should cure in less than 10 seconds at 175-250°C.

There are now non-epoxy based high temperature fill-in paste adhesives that can easily fill-in the vias of 20 micron for such applications. Figure 4 below depicts the TSV structure and the lamination between layers to provide the stress relief.

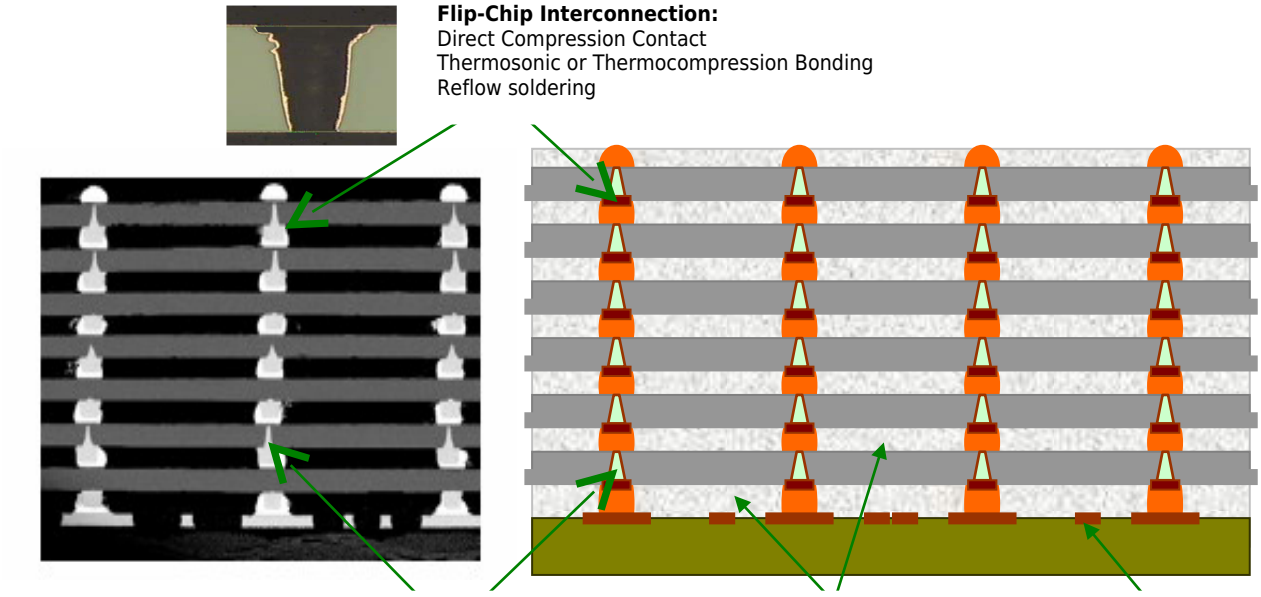


Figure 4: Specialty "fill-in" adhesive and underfill adhesive with low CTE, high modulus and high Tg is essential in the reliability of stack chip packages using through silicon via (TSV) technology.

[3] 3D-TSVs spark packaging revolution; http://images.google.com/imgres?imgurl=http://www.eetasia.com/STATIC/ARTICLE_IMAGES/200809/EEOL_2008SEP01_TPA_MFG_NT_01_VSfig1.jpg&imgrefurl=http://www.eetasia.com/ART_8800541628_480200_NT_10f5ac38.HTM&usg=___MSAelyecPF6X-twJ0Xm91A9RI=&h=386&w=550&sz=48&hl=en&start=23&um=1&itbs=1&tbnid=Fpd0i1uGiLawLM:&tbnh=93&tbnw=133&prev=/images%3Fq%3DTSV%2BSTACK%2BCHIP%26start%3D20%26um%3D1%26hl%3Den%26sa%3DN%26rls%3Dcom.microsoft:en-US%26rlz%3D1I7SUNA_en%26ndsp%3D20%26tbs%3Disch:1

Conclusions:

Wafer level die attach film with very thin bond line had many challenges. Recent advances in die attach materials together with optimized processing conditions overcome these challenges and will enable more advanced technology for packaging semiconductor devices within smaller footprint and volume.

Similarly flip-chip underfill-adhesive can also enable very effective fill-in of the through silicon vias and providing the stress relief between stack chips.