Local Plasma Treatment in a Mask Aligner for Selective Wafer Surface Modification

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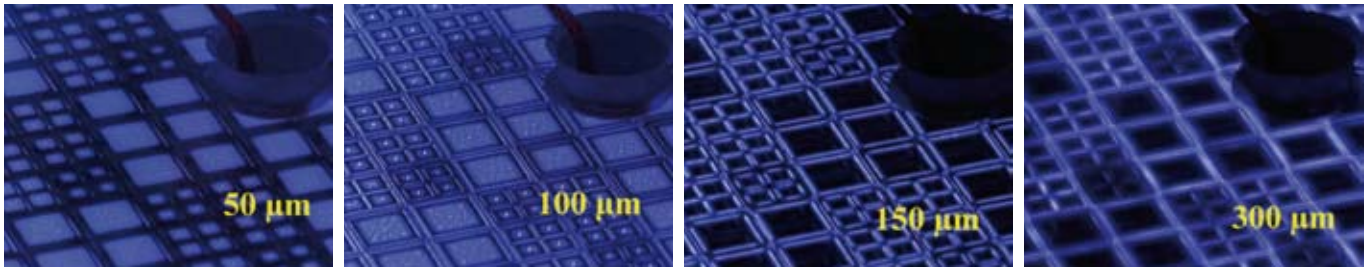

Figure 2:
Local plasma treatment (LPT) of a structured silicon wafer surface. The photographs were taken with different distances between the Si wafer and a transparent counter electrode (ITO on glass), as indicated on the photographs. At low distances, the discharge is limited to the recessed areas of the wafer, at large distances it is concentrated on the protruding ridges of the structure.

Plasma pre-treatment for low-temperature direct wafer bonding is used worldwide in many different applications. In this process the full wafer surface is exposed to the plasma. Recently, a new process for selective plasma treatment has been developed by the Fraunhofer IST and SUSS MicroTec. Micrometer-scale selective area activation and functional layer deposition are the advantages of the process which provide new design and manufacturing options for MEMS/MST applications. The technical realisation is solved by a thin planar electrode in a mask aligner assembly. The plasma process takes less than one minute for all wafer sizes and all relevant mechanical precision parameters of an aligner appear. SUSS MicroTec is about to develop the patented process to industrial maturity and to integrate »Plasma Tooling« into new and used aligners of SUSS as an upgrade kit. The process and the equipment are presented in this paper.

1. Unstructured Plasma Treatment, State of Technology

Plasma treatments are standard applications that are used in the semiconductor industry in many different ways, e.g. for layer deposition, cleaning or etching. Just recently, plasma treatments were more and more employed for plasma surface activation in various MEMS applications. Most of these technologies are based on high frequency low-pressure plasma processes. As an alternative, the ambient pressure plasma treatment can be used. It requires lower investment costs and offers shorter processing times[1, 2, 4]. SUSS MicroTec offers plasma systems for both treatments.

Typically silicon or other semiconductor wafers, as well as glass wafers are treated with plasma in order to activate the surface. This step prepares for the subsequent direct wafer bonding, in order to accelerate the condensation of silanol groups in the bond interface during annealing at moderate and CMOS compatible temperatures. Without plasma pre-treatment bonded silicon wafers would typically need to be annealed at 1100 °C. When activated with plasma the temperature can be lowered down to 400 °C, without comprising the stability of the bond.

In commonly known plasma activation processes the whole wafer area is exposed to the plasma. That is not always necessary. In some cases it can even affect or damage the functionality of the micro components or the electronics.

2. Local Plasma Treatment for Selective Wafer Surface Modification

2.1. Goal of Selective Wafer Surface Modification

In order to enable a selective surface treatment in addition to the full area (unstructured) approach, Fraunhofer IST has now developed a new method for plasma activation at ambient pressure [3, 4, 5]. It provides new design and fabrication possibilities, for example in microfluidic applications, where two or more substrates are supposed to be bonded, in order to develop a functioning chip, in a second step. For simultaneous realization of hydrophilic bond surfaces and hydrophobic channel surfaces the

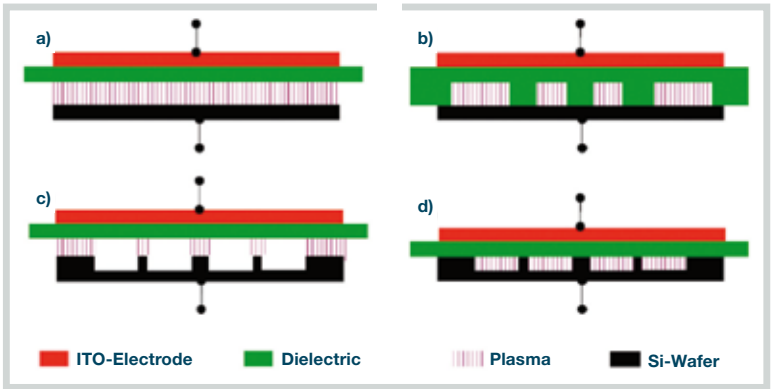

Figure 3:
Different methods of plasma activation
a) full area,
b) selective via structured electrode, c) selective on upper level of substrate,
d) selective in cavities / trenches of the substrate.

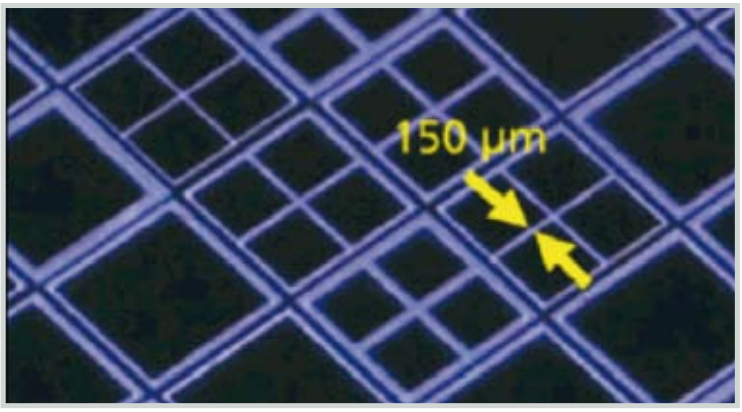

Figure 4:
Selective plasma discharge leads to local modification of the surface properties.

bond surfaces are locally pre-treated in a different way than the micro-channel surfaces.

2.2 Local Plasma Treatment

The application described in this paper is based on the principle of dielectric barrier discharges. For a uniform plasma discharge two electrodes are needed. At least one on them needs to be covered by a dielectric of an adequate thickness leaving a small gas gap between the insulator surface and the counter electrode. The application of an AC voltage in the range of 20 kHz and 5-10 kV leads to a gas discharge which, dependent on the conditions, may be uniform or consist of thousands of microscopically small filaments.

One method of barrier discharge that has already been used for wafer treatment is characterized by two bar-shaped electrodes with an electric potential between them. During treatment chuck and wafer are positioned on ground potential, so that the discharge can be ignited between the electrodes and on the wafer. During plasma scanning of the wafer with the electrodes, the whole wafer area gets exposed to the plasma [1, 2].

However, the new treatment employs a thin, planar electrode, which covers the whole wafer. This new electrode is made of a glass wafer coated with a transparent, conductive layer on the backside. It is now possible to monitor the discharge during treatment. When the planar electrode is adjusted in a small gap opposite to the wafer, it becomes possible to ignite the plasma at an ambient pressure through application of an adequate AC voltage.

How is it possible to treat the wafer just selectively with the plasma?

Therefore, two new treatment methods were developed and will now be described. The first method has been developed for local treatment of wafers with high topography, which can often be found in MEMS/MST applications. When the electrode is adjusted above a wafer with high topography variations, electric fields are generated between the wafer surface and the electrode that show different strengths in the lower and higher areas of the wafer.

When wafer and electrode are brought into contact, the plasma ignites in the cavities (*Figure 3d*) and in larger gaps it flashes on the elevated structures (*Figure 3c*). This means that the already existing structures or topography of a wafer, the electrode gap and the electrode voltage are crucial factors for the final location of the plasma ignition. In this set-up a wafer without topography would get a full surface (unstructured) treatment, as shown in *Figure 3a*.

The second variation of the new treatment has been specially designed for substrates without topography that still need to be treated selectively. Local cavities of the structured electrode are used to limit the formation of plasma to those surface areas that need to be treated (*Figure 3b*). This effect can be additionally supported by local metallization or other structured dielectrics.

Figure 4 shows a snapshot of a process detail from top view during a selective plasma discharge (light areas). A process observation was possible, as for the treatment an electrode coated with a transparent, conductive ITO layer was used. In this application nitrogen was used as process gas.

Figure 5 shows the same wafer detail after treatment. The test with DI water clearly shows changes in the surface tension of the wafer that was made hydrophobic by an HF dip beforehand. Water adheres to those areas that had been treated with plasma, while those that had not been pre-treated remain water-repellent.

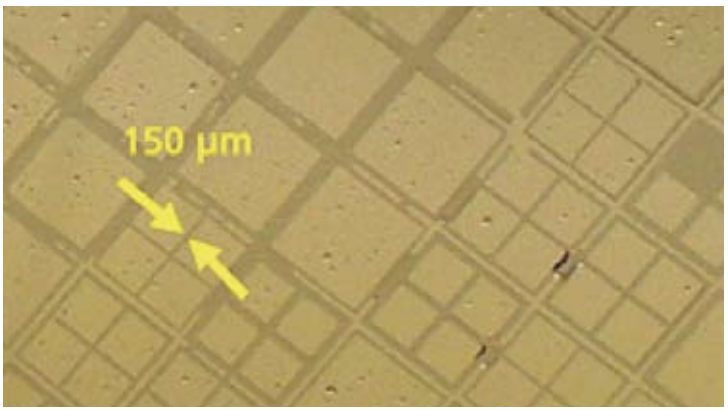

Figure 5:
Local hydrophilization (visualized through wetting with DI water).

3. Local Plasma Treatment – Integration in Mask Aligner

SUSS MicroTec has already started to integrate Local Plasma Treatment into its equipment. The first question that had to be answered was: Do we need to design a completely new system or can we adapt it to already existing technologies? The challenging alignment demands between substrate and electrode made the decision quite easy: the SUSS Aligner (Figure 6) is the systems of choice. Besides, the standard UV-Lithography SUSS MicroTec Aligners can be easily upgraded with addi-

Figure 6: MA/BA6 Mask and Bond Aligner from SUSS MicroTec.

tional functions like bond alignment or nano-imprinting.

In order to be able to employ the bond aligner for the new treatment the following prerequisites need to be fulfilled:

- A dedicated device to integrate a planar electrode and wafer in a parallel set-up
- A mechanism to compensate the wedge error (WEC) between the electrode and the wafer
- Lateral, micrometer precise alignment between electrode and wafer
- Reproducible, micrometer precise gap setting between electrode and wafer

All of these prerequisites are already available in a standard SUSS Aligner. Process relevant modifications refer mainly to the newly designed and exchangeable device for plasma treatment (plasma tooling) and the control software, in order to guarantee the correct process flow.
The relatively high electrode voltage is seen as a critical aspect of integration that affects operator and machine safety. Furthermore, appropriate design set-up, safety inquiries during operation and additional arrangements are concerned. For the process itself the reproducible settings of the electric field between substrate and electrode are crucial and make sure that the discharge really ignites on those areas that are intended to be treated.

The process has to be applicable for conductive, semi conductive as well as for non conductive substrates. In addition the electrode holder and the wafer chuck of the plasma tooling are forming a closed process chamber (mini environment) that enables precise monitoring of the gas atmosphere in the discharge area. Upon applying two process gases at ambient pressure or minor low-pressure, a defined and reproducible process atmosphere is created.

In this process significantly reduced process gases are consumed - compared to existing plasma systems - because of the combination of a relatively small gap between substrate and electrode and the formation of a closed process chamber. Purging gas cycles before and after the plasma process make sure that the operator does not get in touch with the process gas or process gases such as ozone, that can be generated during plasma discharge. The planar and exchangeable electrode is loaded through the loading slide of the MA/BA8 Aligner and transferred automatically to the electrode holder (equivalent to mask holder). The reversible electric contacting of the high voltage electrode as well the electrical isolation of the wafer chuck represents a challenge. During the concept phase of this serious question SUSS MicroTec was supported by Fraunhofer IST with its specific process know-how.
The integration of the new »Plasma Tooling« into the SUSS MicroTec aligner was designed for new and for used machines, that can be retrofitted with the plasma toolkit and opens owners of used SUSS Aligners an easy and cost-efficient way to new plasma treatment. The first system will be installed at Fraunhofer IST in Braunschweig, Germany by the end of the first quarter in 2010.

ACKNOWLEDGEMENTS

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went through vocational training as a certified measure and control technician. Subsequently he studied physics at the Technical University of Braunschweig, where he also received his Diploma. Since 2000 he is research associate in the Atmospheric-Pressure Processes department of the Fraunhofer IST. Presently he is focusing on low-temperature wafer bonding and surface modifications by micro plasmas, the topics of his PhD thesis research.

MARKUS GABRIEL

is product specialist for new wafer bonding business like the temp. bonding and debonding for 3D integration. He has been working for more than 10 years with Suss MicroTec in Germany and USA on various positions. He is member of the SEMI Europe committee on MEMS.