INDIUM CORPORATION®

Indium Corporation Tech Paper

Testing and Prevention of Head-In-Pillow

Authored by Dr. Ning-Cheng Lee and Dr. Yan Liu, Pamela Fiacco, M.S.

Abstract

Head-in-pillow (HIP) is ailing the electronic industry when assembling BGAs or CSPs onto PCBs. It is caused by warpage of components or boards at reflow process, and is aggravated by oxidation. Methods for assessing the potential for occurrence of HIP are highly desired by the industry. Besides using BGA rework station followed by tedious dye and pry treatment, two other simpler methods are introduced in this work, Tiny Dot Paste method and Ball Onto Paste method. The tiny Dot Paste method is stressed on the assessment of oxidation barrier capability of solder paste, while Ball Onto Paste method assesses combined capability of oxidation resistance and excessive fluxing capacity. Both methods are quick, easy, and close simulation, with the latter being better in real process simulation. Prevention of HIP can be accomplished by (1) designing packages without warpage, (2) printing more paste, (3) dipping solder paste or flux, (4) using inert reflow atmosphere, (5) reducing reflow temperature, (6) placing heat shield on BGA or CSP, (7) avoiding using water soluble solder paste for BGA bumped with no-clean process, (8) using solder bumps or solder powder with oxidation resistant alloy, (9) using fluxes with high oxidation barrier capability and high fluxing capacity. Among all options listed above, using solder paste with high oxidation barrier capability and high fluxing capacity is considered the most easily implemented approaches.

Key Words: Head-in-pillow, solder, soldering, reflow, SMT, solder paste, BGA, CSP

Introduction

The electronic industry is moving toward smaller, faster, and cheaper. In the case of CSP or BGA, the components are reducing in pitch and ball size but increasing in package size. Due to the high complexity in design, many components inevitably suffer from warpage at soldering temperature, and consequently result in head-in-pillow (HIP) defect, as exemplified in Fig. 1. The symptom of this defect is that the solder ball on BGA is sitting on solder dome formed from coalescence of solder paste. Although mechanical contact is established, solder joint is neither formed metallurgically nor exhibiting an adequate joint shape. Furthermore, electrical continuity may or may not be established. This defect type is a liability of devices, and is recognized to be related to type

DR. NING-CHENG LEE

Dr. Ning-Cheng Lee, Vice President of Technology, Indium Corporation, is a world-renown soldering expert and an SMTA Member of Distinction. He has nearly 30 years of experience in the development of fluxes and solder pastes for SMT industries. He has extensive experience in the development of high temperature polymers, encapsulants for microelectronics, underfills, and adhesives.

email: drlee@indium.com

Full biography: indium.com/corporate/bio/ning-cheng_lee.php

A **QR** (quick response) **code** contains encoded data.

When scanned with a smart phone's camera (via a QR reader application), it will take you to a specific URL or text message.

- *Download article*
- *Share with a friend*

indium.us/D152

Form no. 98672

of components, processes, and solder pastes. However, as of today, an effective testing method has not been reported for predicting the propensity of HIP phenomenon under a given combination of process and materials. This becomes a desperate need when a robust solder paste is desired at solder paste selection phase. In this work, test methods have been developed for assessing the potential of having HIP issue for a specific solder paste. In the meantime, mechanisms of formation of HIP are also discussed. Accordingly, new solder pastes with excessive resistance against HIP were developed and assessed with these test methods, with results to be discussed in detail.

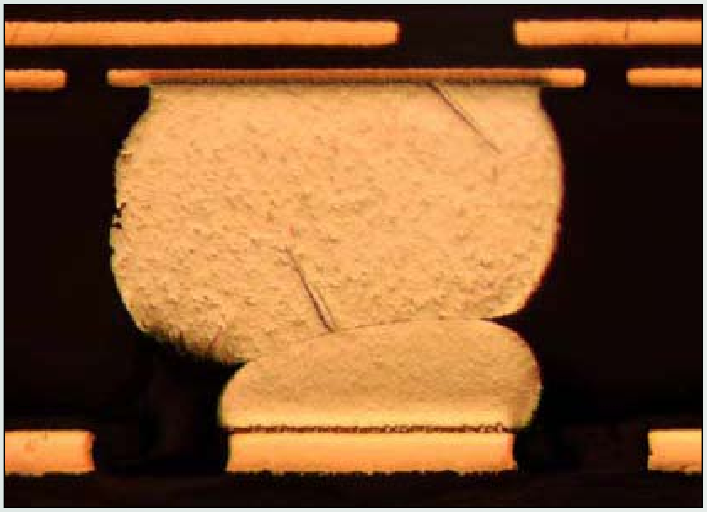


Fig. 1 Example of head-in-pillow defect.

Mechanism of Formation

The mechanism of formation of HIP can be illustrated in Fig. 2. Due to mismatch in thermal expansion coefficient, certain BGA or CSP packages, or sometimes the PCB itself, tend to warp upon heating. At board level assembly stage, this warpage may result in separation between solder paste and solder bump. Further heating results in the melting of the separated paste and solder bump, as shown in the middle drawing. Upon cooling, the warpage gradually diminishes and eventually re-establishes contact between solder bump and solder dome formed from coalesced solder paste. If the warpage is very significant, the solder may solidify before contact, and inevitably fail to form a proper coalesced solder joint. In some instances, both sides may be in liquid state upon contact, but still fail to coalesce. This is mainly attributable to the separation of liquid solder moiety by the solder oxide film developed during heating or prior mishandling.

Package Warping Assessment

The propensity of a BGA or CSP to warp can be assessed by profiling the package warpage under thermal exposure similar to solder reflow conditions using shadow moiré techniques [1-3]. An alternative, qualitative, quick and simple way is to place the BGA on a glass plate with bump side downward. This BGA/glass plate is then sent through oven using the reflow profile as BGA assembly, followed by examining the bump shape. If the perimeter or center bumps flattened much more than the rest bumps, then significant warpage has occurred during heating, and chance for HIP to happen on this package is relatively high.

Inducing HIP

HIP symptoms can be created by running regular production assembly processes. However, since HIP occurring rate is not very high in most cases, this approach is unacceptable due to its high cost. Accordingly, a method which will amplify the HIP defect rate is desirable for assessing the HIP propensity.

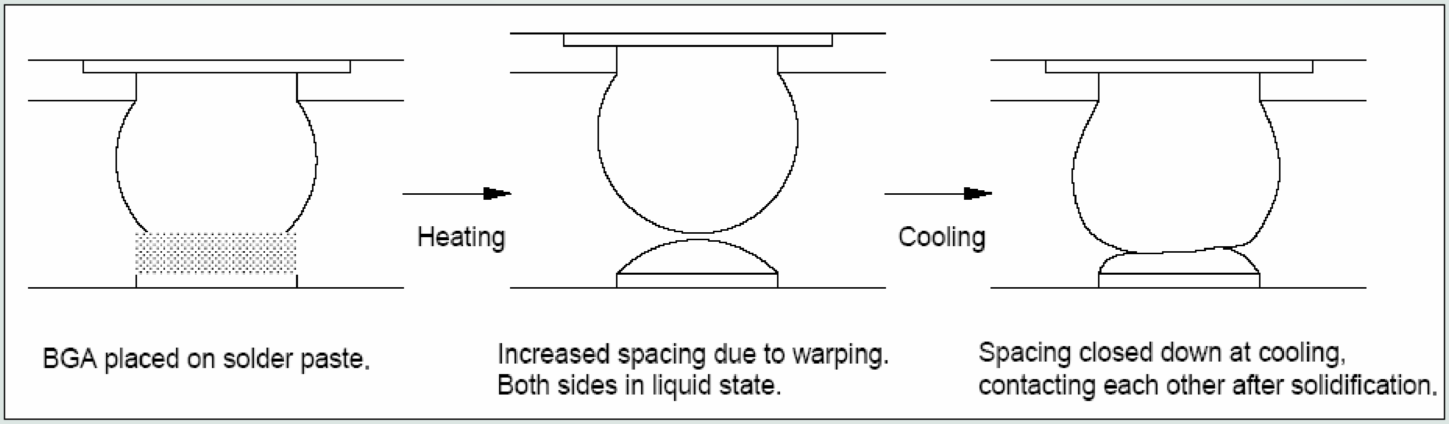


Fig. 2 Formation mechanism of HIP.

BGA Rework Station

One way to induce HIP is through the use of BGA rework station, as practiced by some assembly houses. Here both BGA and printed paste on PCB are held under hot air through various stage of reflow profile before BGA is placed onto the coalesced paste. After completing the full reflow cycle, the assembled BGA is then examined for evidence of HIP. In general, X-ray is not very sensitive for catching HIP, and dye and pry method is needed for assessing HIP propensity. Overall, this rework station method is fairly effective in HIP potential assessment, but also is quite tedious.

Tiny Dot Paste

Since solder oxide film is a major contributor to HIP defect, factors aggravating solder oxide formation would serve as a good acceleration factor for HIP. A small dot of solder paste has high surface area per unit volume, thus is very sensitive to oxidation. Based on this consideration, Tiny Dot Paste method was devised, with test procedure described below.

1. Print solder paste onto pads, with pad dimension specified below. Stencil used is 127 µ in thickness, with opening being the same as pad dimension. Pads are circular, with the following NSMD OSP pad/pitch dimension (see Fig. 3).
   245 µ / 600 µ
   325 µ / 800 µ
   406 µ /1000 µ
2. Reflow through SS (short soaking) and LS (long soaking) profiles under air (see Fig. 4).
3. Examine under 40X microscope for graping performance. Fig. 5 demonstrates bumps with graping and bumps without graping.
4. LS profile with smaller deposit is more vulnerable toward graping/HIP.
5. The graping symptom of pastes can be ranked accordingly.
6. The one with least graping is also the one most resistant toward HIP.

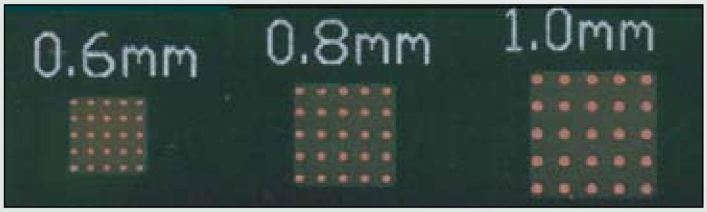


Fig. 3 NSMD OSP circular pads, with pad/pitch dimension being 245µ/600µ, 325µ/800µ, and 406µ/1000µ, respectively.

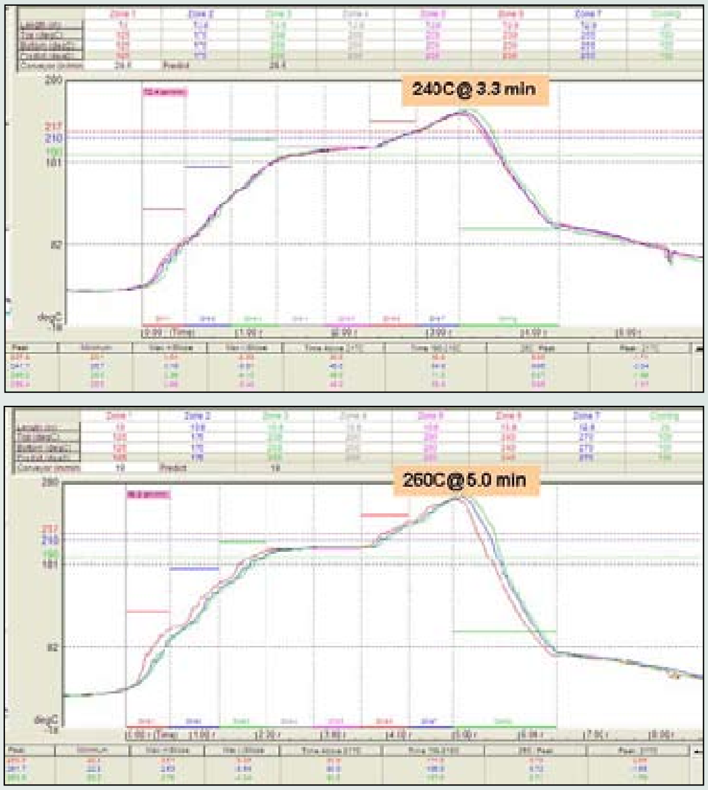


Fig. 4 SS (short soaking, top) and LS (long soaking, bottom) profiles used in Tiny Dot Paste method.

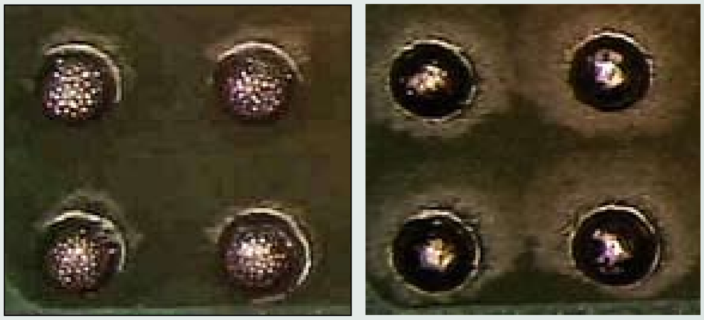


Fig. 5 Bumps with graping (left) and without graping (right).

The Tiny Dot Paste method is very easy to implement, and is very informative. The limitation of this method is that only oxidation of solder paste is evaluated, and the impact of bump oxidation is not included.

Ball Onto Paste

In this method, both paste and solder ball are subjected to oxidation prior to putting them together. Fig. 6 shows the schematic drawing about the test method, which can be described with the following procedure. The solder ball alloy should be the same as BGA ball alloy.

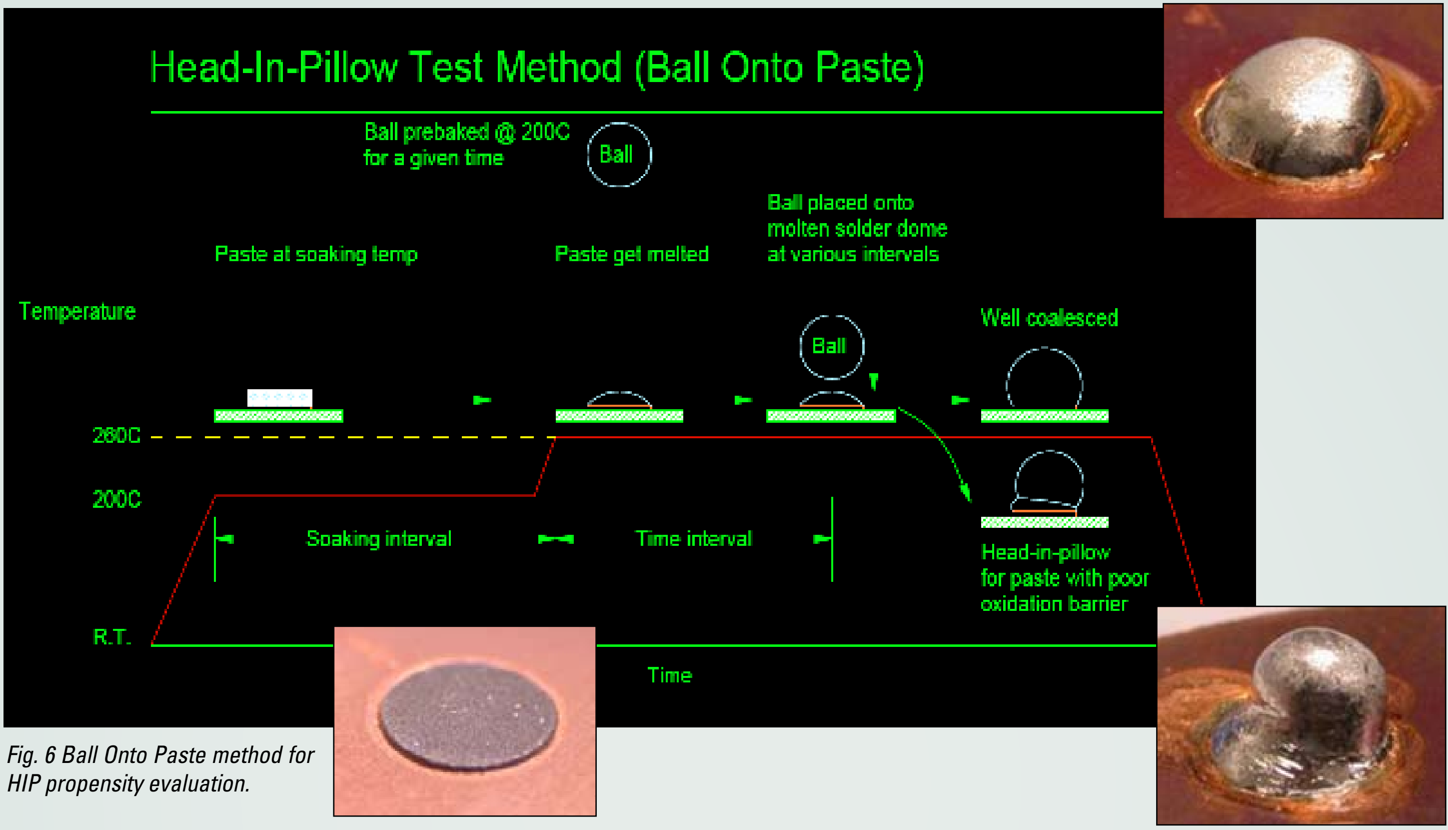


Fig. 6 Ball Onto Paste method for HIP propensity evaluation.

1. Precondition 2.3 mm diameter solder ball at 200°C for a given time (e.g. 25 min.), then put it aside.
2. Print 3.0 mm diameter solder paste onto Cu coupon using a 125 µ thick stencil. Precondition the printed solder paste at 200°C on hot plate, with time varies (e.g. 1, 2, 3, 4 min.).
3. Move the preconditioned specimen onto a 260°C hot plate.
4. Once the paste melted, hold the coalesced solder at 260°C, with time varies (e.g. 0, 20, 60, 80 seconds).
5. Drop a preconditioned solder ball onto the liquid solder dome. Hold the specimen on the 260°C hot plate for 20 more seconds. Remove specimen from hot plate.
6. Examine the specimen under 40X optical microscope for incomplete coalescence, which reflects propensity of HIP.

Example of printed paste (lower left), full coalescence between ball and paste (upper right), and partial coalescence (lower right) are demonstrated in Fig. 6

With oxidation of solder ball and solder paste (both prior to melting and after melting) being regulated, this test method essentially fully simulates the impact of oxidation factor on HIP propensity. It should be pointed out that oxidation resistance of solder paste is able to assure the proper reflow of solder paste, but not able to assure oxide removal for solder bump. Bump oxide removal actually relies on the excessive fluxing capacity of solder paste. By introducing solder ball oxidation as one variable, this test method assesses combined capability of oxidation resistance and excessive fluxing capacity. The merit of Ball Onto Paste method is quick, easy, and close simulation, without the need of BGA rework station and the tedious dye and pry procedure.

Prevention of HIP

With several valid test methods established, it is time now to look into what can be done to prevent HIP from happening, and the effect of proposed solutions can be verified easily with the test methods.

Design

Check the warping extent of BGA/CSP components or boards. Try to avoid selections of components/boards which are prone to warp, or get back to component/board supplier to eliminate or reduce the warpage by design, such as stiffening up the component by adding more Cu ground layer in package.

Process

For HIP occurring at perimeter of package, print more paste on the perimeter so that (1) the coalesced paste can reach higher to get in contact with solder bump, (2) paste has less oxidation and more flux capacity for cleaning up the oxidized bump. Dip BGA into flux bed or dippable solder paste bed, then place onto printed paste on BGA footprint. The additional flux or paste volume will reduce the impact of oxidation. For HIP occurring at center of package, flux or paste dipping is recommended.

HIP could also be caused by using water soluble solder paste for assembling BGA bumped with no-clean process. A no-clean process will always have a no-clean flux residue film left on the surface of solder bump, and no-clean flux residue is always hydrophobic in nature in order to prevent leakage current. On the other hand, water soluble solder paste is always hydrophilic in nature in order to be soluble in water. A hydrophilic flux will have great difficulty to penetrate through a hydrophobic flux residue film on solder bump due to the significant difference in polarity, and consequently result in HIP. Therefore, if a no-clean bumped BGA/CSP package is selected, a no-clean solder paste and/or no-clean dip flux should be selected at board level assembly.

If HIP occurs randomly, excessively oxidized ball at ball bumping stage is the primary cause. Change ball bumping process to first-in-first-out process will eliminate the problem. Or, the oxidation resistance of ball should be improved with either organic or inorganic protection treatment. On the other hand, HIP can also be achieved by using oxidation resistant solder alloys, such as solder alloys doped with P or Ge.

Modify reflow profile so that the time at elevated temperature is reduced, particularly at soaking stage. Under all instances, changing reflow atmosphere to inert atmosphere will always help.

On the other hand, reducing the temperature of warped component will help directly. This can be achieved by reducing the reflow temperature setting, or by adding heat shield to the specific component, particularly when the BGA is not a relatively large component on the board.

Material

Perhaps use of solder paste with high oxidation resistance will be the easiest way to prevent occurrence of HIP. This oxidation can be achieved via flux resistant toward burn-off at soldering process. This is particularly critical since the amount of solder paste or flux deposited reduces rapidly due to miniaturization.

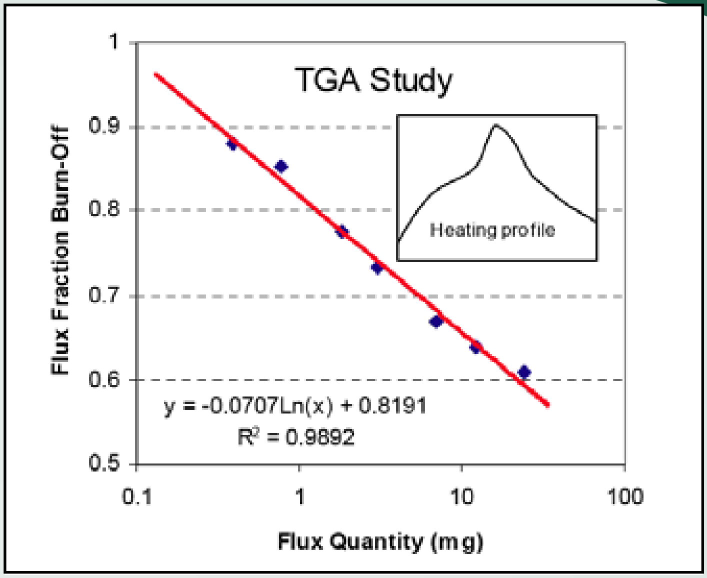
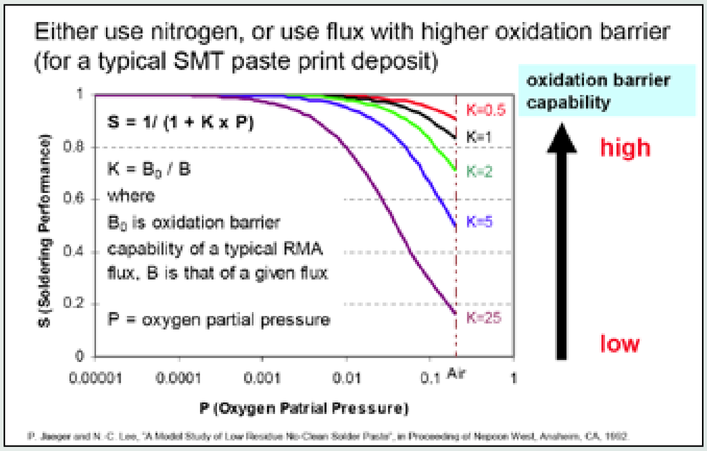


Fig. 7 Flux burn-off increases with decreasing flux deposit quantity.



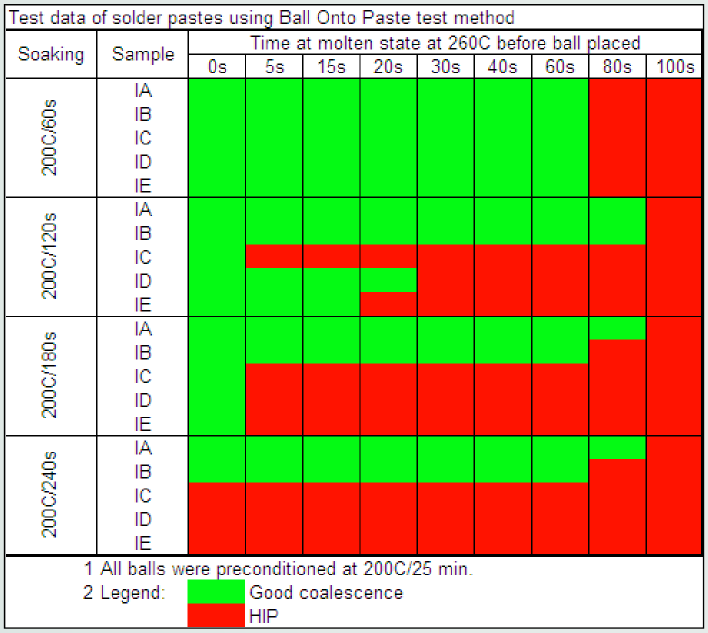
P. Jaeger and N.-C. Lee, "A Model Study of Low Residue No-Clean Solder Paste", in Proceeding of Nepcon West, Anaheim, CA, 1992.

Fig. 8 Soldering performance increases with increasing oxidation barrier capability.

A smaller deposit has a higher surface area per unit volume, and consequently suffers a higher burn-off problem, as shown in Fig. 7. Results here clearly show that nearly 90% flux burnt off when the flux quantity is tiny. Apparently, high flux burn-off behavior will leave less amount of flux to remove the oxide, and inevitably will aggravate problems of HIP.

Besides resistance against flux burn-off, oxidation barrier capability of flux is equally or even more important in preventing HIP. With a low oxidation barrier capability, solder powder or metal parts covered by flux can be easily oxidized at soldering. Unless costly inert reflow atmosphere is adopted, this inevitably will result in HIP. The higher the oxidation barrier capability, the less the need of an inert reflow atmosphere in achieving a satisfactory solder joint, as illustrated in Fig. 8.

Fig. 9 Results of Tiny Dot Paste test on solder pastes with various oxidation barrier capability.



Test data of solder pastes using Ball Onto Paste test method

Soaking	Sample	Time at molten state at 260C before ball placed								
		0s	5s	15s	20s	30s	40s	60s	80s	100s
200C/60s	IA	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟥
	IB	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟥
	IC	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟥
	ID	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟥
	IE	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟥
200C/120s	IA	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥
	IB	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥
	IC	🟩	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥
	ID	🟩	🟩	🟩	🟩	🟥	🟥	🟥	🟥	🟥
	IE	🟩	🟩	🟩	🟥	🟥	🟥	🟥	🟥	🟥
200C/180s	IA	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥
	IB	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟥
	IC	🟩	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥
	ID	🟩	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥
	IE	🟩	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥
200C/240s	IA	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥
	IB	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟥
	IC	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥
	ID	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥
	IE	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥	🟥

1 All balls were preconditioned at 200C/25 min.

2 Legend: 🟩 Good coalescence
🟥 HIP

Fig. 10 Results of Ball Onto Paste test for solder pastes IA to IE.

The effect of oxidation barrier capability of flux on HIP is well demonstrated with either Tiny Dot Paste method or Ball Onto Paste method. Fig. 9 shows the testing results of Tiny Dot Paste when comparing a series of solder pastes A to J with various level of oxidation barrier capability. Sample I was formulated to exhibit a particularly high oxidation barrier capability, while other pastes were regular SMT solder pastes. The superior non-graping performance of sample I strongly indicates the importance of oxidation barrier capability.

Fig. 10 shows the results of Ball Onto Paste testing when comparing a series of specially formulated pastes IA to IE. The ranking of oxidation barrier capability is IA, IB > IC, ID, IE. Although some data scattering can be discerned, in general the HIP symptom worsens with increasing soaking time at 200°C, and pastes with high oxidation barrier capability correlate well with low propensity in HIP occurrence.

Among all options listed above, using solder paste with high oxidation barrier capability and high fluxing capacity is considered the most easily implemented approaches.

Conclusion

Head-in-pillow (HIP) is ailing the electronic industry when assembling BGAs or CSPs onto PCBs. It is caused by warpage of components or boards at reflow process, and is aggravated by oxidation. Methods for assessing the potential for occurrence of HIP are highly desired by the industry. Besides using BGA rework station followed by tedious dye and pry treatment, two other simpler methods are introduced in this work, Tiny Dot Paste method and Ball Onto Paste method. The Tiny Dot Paste method is stressed on the assessment of oxidation barrier capability of solder paste, while Ball Onto Paste method assesses combined capability of oxidation resistance and excessive fluxing capacity. Both methods are quick, easy, and close simulation, with the latter being better in real process simulation. Prevention of HIP can be accomplished by (1) designing packages without warpage, (2) printing more paste, (3) dipping solder paste or flux, (4) using inert reflow atmosphere, (5) reducing reflow temperature, (6) placing heat shield on BGA or CSP, (7) avoiding using water soluble solder paste for BGA bumped with no-clean process, (8) using solder bumps or solder powder with oxidation resistant alloy, (9) using fluxes with high oxidation barrier capability and high fluxing capacity. Among all options listed above, using solder paste with high oxidation barrier capability and high fluxing capacity is considered the most easily implemented approaches.

Reference

1. David W. Garrett, *“Elevated temperature measurements of warpage of BGA packages,”* http://www.akrometrix.com/whitepapers/

2. Y. Y. Wang and P. Hassell, *“Measurement of thermally induced warpage of BGA packages/substrates using phase-stepping shadow moire,”* Electronic Packaging Technology Conference, 1997. Proceedings of the 1997 1st.

3. Xiaoyuan He and Sheng Liu, *“Real time warpage measurement of a plastic BGA by projected grating method,”* International symposium on microelectronics: (San Diego CA, 1-4 November 1998) (01/11/1998) 1998, vol. 3582, pp. 537-542. First presented at ECTC, sponsored by IEEE, June 2010, Las Vegas, NV.

First published at ECTC, sponsored by IEEE, June 2010, Las Vegas, NV.