WAFER LEVEL PACKAGING OF COMPOUND SEMICONDUCTORS

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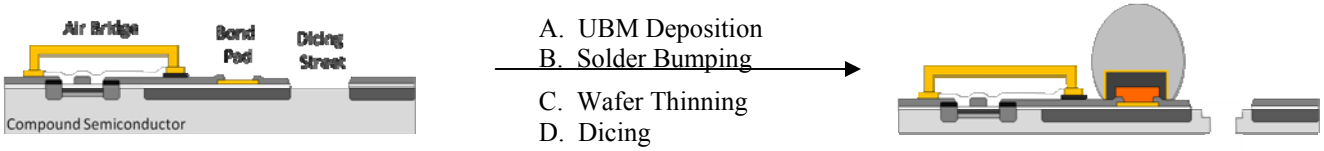
ABSTRACT
The microelectronics industry has implemented a number of different Wafer Level Packaging (WLP) technologies for high volume manufacturing, including: UBM deposition, solder bumping, wafer thinning, and dicing. These technologies were successfully developed and implemented at a number of contract manufacturing companies, and then licensed to many of the semiconductor manufacturers and foundries. The largest production volumes for these technologies are for silicon-based semiconductors. Continuous improvements and modifications to these WLP processes, have made them compatible with the changes observed over the years in silicon semiconductor technologies. These industry changes include: the move from aluminum to copper interconnect metallurgy, increases in wafer size, decreases in pad pitch, and the use of low-K dielectrics. In contrast, the direct transfer of these WLP technologies to compound semiconductor devices, like GaAs, SiC, InP, GaN, and Sapphire; has been limited due to a number of technical compatibility issues, several perceived compatibility issues, and some business concerns [1-4].



From a technical standpoint, many compound semiconductor devices contain fragile air bridges, gold bond pads, topographical cavities & trenches, and have a number of unique bulk material properties which are sensitive to the mechanical and chemical processes associated with the standard WLP operations used for silicon wafers. In addition, most of the newer contract manufacturing companies and foundries have implemented mostly 200 and 300mm wafer capabilities into their facilities. This limits the number of places that one can outsource the processing of 100 and 150 mm compound semiconductor wafers.

From a perception point-of-view, companies which are processing large numbers of silicon based semiconductor wafers at their facilities, are reluctant to process many of these compound semiconductors because there is a perceived issue with cross contamination between the different wafer materials. Companies are not willing to risk their current business of processing silicon wafers by introducing these new materials into their existing process flows.

From a business perspective, many companies are reluctant to take the liability risks associated with some of the very high-value compound semiconductors. In addition, the volumes for many of the compound semiconductor devices are very small compared to silicon based devices, thus making it hard to justify interruption in the silicon wafer flows to accommodate these lower volume products.

In spite of these issues and perceptions, the markets for compound semiconductors are expand. Several high profile examples include: the increasing number of frequency and power management devices going into cell phones, light emitting diodes, and solar cells [5].

The strategy for the work described in this paper, is to protect all structures and surfaces with either a spin-on resist or laminated film during each step in the process flow. These layers will protect the wafer from mechanical and chemical damage, and at the same time, protect the fab from contamination by the compound semiconductor.

INTRODUCTION

The test vehicle in this study is a GaAs device which contains both gold air-bridges (3µm tall) and gold bond pads. The wafer is 4 inches in diameter and 600 µm thick. The dicing streets and wafer backside are non-passivated. The active portion of the die is passivated with 0.6 µm of Si_3N_4. The bond pads are defined by 150 µm diameter openings in the passivation (Figure 1).

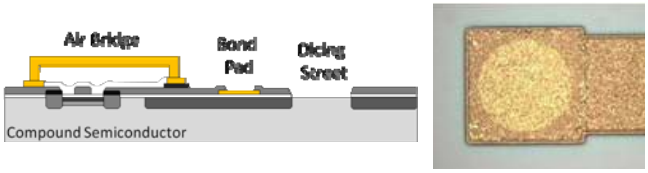


Figure 1. a. Schematic drawing of GaAs test vehicle, and b. an optical image of a gold bond pad on the GaAs device.

This paper describes the process details of the Wafer Level Processes used to convert the GaAs test wafer into

individual die: UBM deposition, solder bumping, wafer thinning, and dicing. The criteria (or processing rules) which were considered when selecting the specific technologies and process flows for the WLP operations include:

Processing Rules

- No metals directly deposited onto air bridges (residuals)
- No mechanic contact with wafer top (damage air bridges)
- No ultrasonics (wafer damage)
- No exposure to corrosive etch chemicals (acid or base)
- No plasma processes (etch passivation)

In order to comply with these rules, a series of spin-on resists and film lamination processes were used to protect both the wafer from damage and the fab from cross-contamination during the processing. The following is an outline of all the individual process steps performed in this study, including the resist and laminate operations.

Process Flow

A. UBM Deposition
   Deposit Ti/Cu Cap Metal
      1. Coat and Pattern Liftoff Resist
      2. Sputter Deposit Ti/Cu
      3. Strip Resist
   Ni/Au UBM Deposition
      4. Coat and Pattern Frontside Resist
      5. Laminate Backside Film
      6. Plate Electroless Nickel and Gold
      7. Remove Backside Film
      8. Strip Frontside Resist

B. Solder Bumping
      9. Transfer Solder Spheres (or alternatively Jet)
      10. Hot Plate Reflow

C. Wafer Thinning
      11. Spin-On Frontside Resist
      12. Laminate Film to Frontside
      13. Grind and Polish Wafer
      14. Remove Laminate Film

D. Dicing
      15. Laminate Film to Backside
      16. Remove Frontside Resist
      17. Saw Wafer (Dual Cut)

UBM Deposition (Deposit Ti/Cu Cap Metal)
Solder cannot be deposited directly onto the gold bond pads because the gold would be partially consumed during the solder reflow process, and will eventually fail in the field due to thermal and electro-migration processes. An under-bump-metallization (UBM) is required to keep these destructive processes form occurring. Note: This is true for all silicon based semiconductors as well.

There are several options for depositing the UBM on the wafer, including: sputter deposition followed by a subtractive wet chemical etch, electroplating, or electroless plating. None of these are directly transferable to GaAs devices while still observing the five technical rules as described above. For example, the use of a thin film sputtering process, followed by subtractive etching of the metal layers, requires that all surfaces of the wafer be coated with metal and then selectively etched with either caustic or acidic chemicals. There are a number of opportunities for degradation of both the air bridges and various semiconducting materials using this subtractive sputtering method.

One will encounter many of these same interactions, which can damage or destroy the GaAs device, by using electroplating technologies to form the UBM. The use of an electroless nickel/gold plating process (ENIG), unfortunately, will not initiate on the gold bond pads, and therefore, is also not directly compatible with GaAs devices with gold bond pads. In addition, some of the chemicals in the ENIG process will damage the device.

In this study, a combination of resist deposition, thin film sputtering, and electroless nickel/gold technologies were used to create the UBM. To convert the gold surface of the bond pad over to a metal which is compatible with the electroless nickel/gold process, thin layers of titanium and copper were first sputtered onto the GaAs wafer using a liftoff process. The use of a liftoff process has the advantage over a subtractive etch process, in that the liftoff resist protects the whole wafer from chemicals and mechanical damage [6].

A standard positive photoresist was coated onto the wafer using standard spin coating equipment, soft baked on a hot plate, and flood exposed. This layer was approximately 3-4 μm in thickness. A second layer of photoresist was coated on top of the first resist layer. This layer was then pattern exposed and batch developed to open up the area above the bond pad (155 μm). By controlling the develop time, the bottom layer (which was flood exposed) will also be developed to create a slightly larger diameter opening (<175 μm).

Step A1: Deposit and pattern a dual layer liftoff resist (Suss MA200 photolithography tool).

The resist stack was then baked to make it stable to the subsequent sputtering process. All films which were baked in the range of 100 ºC to 200 ºC were found to be stable to the sputtering process.

The sputtering of Ti and Cu was accomplished using a standard magnetron sputtering tool that was capable of RF pre-sputtering the wafer with argon and was also equipped with a chilled wafer platen [7]. After Argon plasma pre-cleaning, 500 Å of Ti was deposited on top of the gold to create both an adhesion layer and diffusion barrier. A 6000 Å layer of copper was then sputtered on top of the Ti layer. The thickness of this Cu layer must be thick enough to be stable in the subsequent electroless plating steps and thin enough not to create a metal bridge between the liftoff resist layers.

Step A2: Sputter deposit 500 Å of Ti followed by 6000 Å of Cu (Perkin Elmer 2400 sputtering tool).

One of the most critical process parameters in the sputtering process is to keep the sputtering power low. The following figures show the results of sputtering at high powers and that of films sputtered at lower powers.

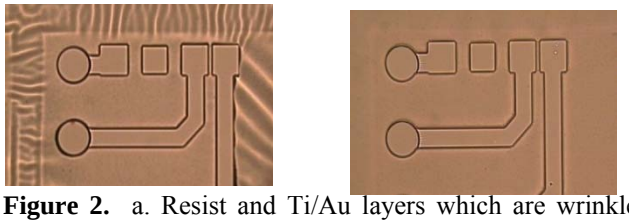
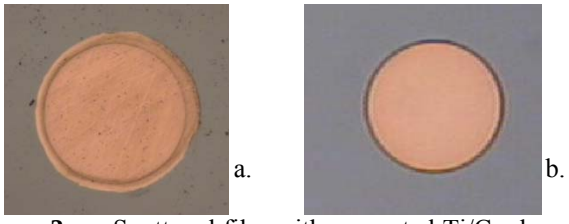


Figure 2. a. Resist and Ti/Au layers which are wrinkled using sputtering power over 1500W, and b. smooth resist and Ti/Au using lower sputtering power (≤1000W).

In addition, because sputtering is not a true line of sight deposition process there is a tendency for the sputtered metals to deposit under the top resist, creating a thin layer of Ti/Cu that can be nearly equal to the diameter of the opening in the bottom resist.



a. b.

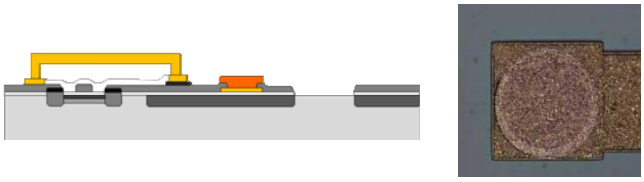
Figure 3. a. Sputtered film with unwanted Ti/Cu deposited under the top resist layer, and b. Ti/Cu film after process optimization.

Optimization is accomplished by controlling the sputtering power, gas pressure, throw distance, and resist layer thicknesses. The alternative to sputtering is to use an evaporation technique which is a true line-of-sight PVD process.

Table 1. Parameters used for Ti/Cu sputtering.

	Ti Layer	Cu layer
Gas/Pressure	Argon: $5x10^{-3}$ Torr	Argon: $5x10^{-3}$ Torr
Sputter Mode	Biased	Biased
Power	500 W	1000 W
Time	5 min (500 Å)	42 min (6000 Å)

The films that were baked at 100 ºC were found to be easily stripped after sputtering, using either acetone at room temperature or NMP at 65ºC. Films baked at higher temperatures took longer to strip or required elevated temperatures to strip. The use of ultrasonics to expedite this liftoff process was found to cause catastrophic damage to the GaAs test wafer; typically shattering the whole wafer.



Step A3: Strip the liftoff resist from the wafer.

The sputtering process is typically characterized for quality by measuring the height uniformity across the wafer and by measuring the adhesion to the underlying materials (Au and Si_3N_4).

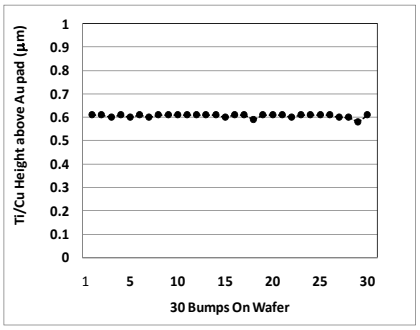


Figure 4. Plot of Ti/Cu sputtered height on 30 pad locations across the wafer (Tencor profilometer).

The sputtering uniformity across a 100 mm wafer is fairly tight. The sputtering target in the tool used in this study is 9 inches in diameter. The wafer platen rotates under the sputtering target, which also increases the sputtering uniformity.

UBM Deposition (Ni/Au UBM Deposition)
The electroless nickel and gold plating process is often described in the literature as selective. This is true for most silicon wafers where all the structures are protected by a thick silicon nitride passivation. GaAs devices have many exposed metals and doped areas where nickel can initiate and plate. These areas need to be protected by a material which is easily applied, can survive the aggressive chemistries in the plating line, and be easily removed; all

without damaging the air bridges or affecting the exposed GaAs on the wafer.

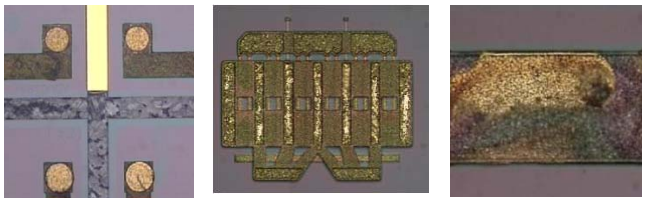


Figure 5. Examples of spurious Ni/Au plating on an unprotected GaAs device: a. in the scribe streets, b. on air bridges, and c. in pinholes in the thin passivation over metal traces.

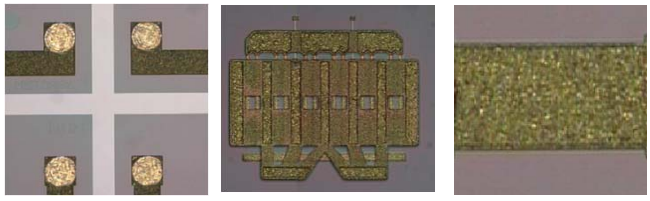


Figure 6. Examples of no spurious Ni/Au plating on a resist protected GaAs device: a. scribe streets, b. air bridges, and c. passivation over metal traces.

A large number of resists were evaluated for this top side protection coating. Only a select few were found to survive the electroless nickel process and still be easily removed in a benign solvent. All of the novalac based resists that we evaluated required a very hard bake at ~200 ºC in order to survive the electroless plating process. Removal of this resist requires very harsh chemicals, or alternatively, plasma ashing which both damage the wafer.

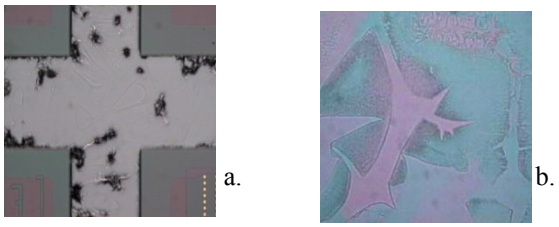


Figure 7. Examples of damage to: a. the GaAs dicing streets, and b. passivation, using piranha etch chemicals and/or plasma ashing to strip the resist.

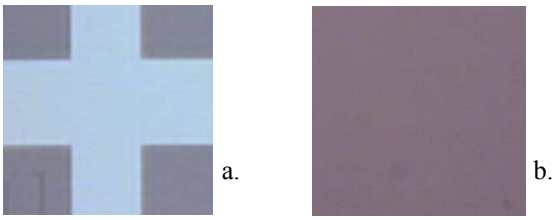
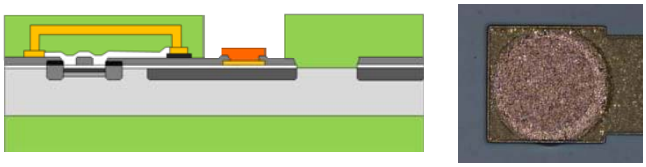


Figure 8. Examples of a. undamaged streets and b. passivation using acetone or NMP to strip the resist.

In addition to protecting the front side of the wafer, the backside needs protection from the electroless plating chemicals as well. A UV release film was laminated onto the backside of the wafer to protect the backside from spurious plating.



Steps A4 and A5: Deposit and pattern a protective resist on the frontside (160 µm opening) and then laminate a UV release film on the backside of the wafer (Suss Microtech MA200 and Ultron Laminator).

The electroless nickel/gold plating process is carried out using an automated plating line which sequentially processes the wafers through a series of chemical baths and rinse stations [8-9].

Wet Chemical Process
Cassette Based Transport
PLC Controlled
50-100 8”wfrs/hr
100-200 4”wfrs/hr
NiAu or NiPdAu
Cu or Al Based ICs
Auto Chemical Analysis
Auto Chemical Replenish
Auto Wafer Dry

Figure 9. Electroless Nickel Plating Line (PacTech PacLine-3000).

The first bath in the plating sequence is a dilute acid used to clean the Cu pads of any residual organic or silicon based contaminates. The second step is to remove any native oxide that may have built up on the copper pad surface. This is performed using a much stronger etching solution. The next step is to activate the surface of the copper using a palladium catalyst. This is followed by immersion in a nickel sulfate based plating bath and then an immersion gold plating bath. A nominal nickel height of 3 microns and a 500 Å layer of gold were deposited in this study.

Step A6: Electroless plating of 3 µm Nickel and 500 Å Gold (PacTech PacLine-3000).

The laminate film on the backside of the wafer was removed by first exposing the film to UV radiation and then peeling off the film. The thin film resist on the frontside was

removed by immersion in acetone at RT or using an NMP based solvent at 65ºC.

Steps A7-A8: Expose and remove backside laminate film, and strip the frontside resist (Ultron UV exposure tool).

The electroless nickel gold plating process is typically characterized for quality by measuring the height uniformity across the wafer and by measuring the adhesion to the copper pad.

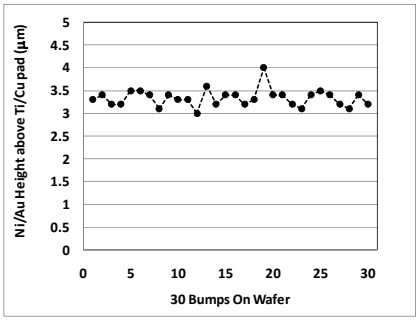
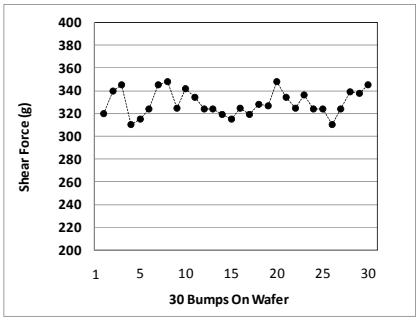


Figure 10. Plot of Ni/Au plating height on 30 pad locations across the wafer (Tencor profilometer).



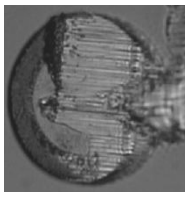


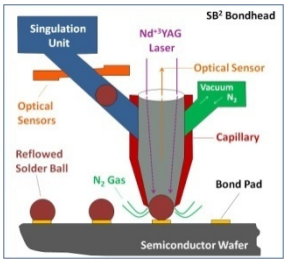
Figure 11. Plot of shear force on 30 pad locations across the wafer plated with 25 µm tall Nickel (Dage shear tool).

Tall nickel/gold structures (25 µm) were deposited on several wafers to evaluate the Ni to Cu adhesion. For all of the pads which were sheared, the mode of failure was in the Au pad metallurgy, circuitry below the bond pad, or fracturing of the GaAs (no e-Ni to Cu failure). This indicates that the adhesion of Ni to Cu is not a limiting factor in the metal stack. In addition, it also suggests that the adhesion of the Ti to Au, and Cu to Ti is also good.

Solder Bumping

Some of the same concerns about mechanical and chemical degradation during UBM deposition are also relevant to the operations related to solder bumping. Several options exist for solder bumping, including: paste printing, electroplating, or PVD [10]. Each of these technologies would also require a unique set of resists to protect the GaAs structures from damage during processing. In this study, two different techniques were evaluated which did not require a protective resist layer: a laser based bumping process which drops a single solder sphere onto the bond pad and then laser reflows the solder just as it reaches the pad [11-13], and a solder sphere transfer process which places all the solder spheres onto the wafer at once [14-16].

The laser based single-sphere process has no mechanical contact with the wafer and is fluxless, thus eliminating any chemical interactions with the device or need for protective resists. Solder bumps using this technique are deposited at a rate of 6-10 spheres per second. This technology has been used successfully for many applications, but is most useful for low volume products, prototyping, or products with low I/O count. Preformed solder spheres in the range of 80 to 760 µm are compatible with this technology. All solder alloys can be deposited with this system by adjusting the laser power and pulse width. For this study, SnPb Eutectic spheres were used which were 150 µm in diameter.



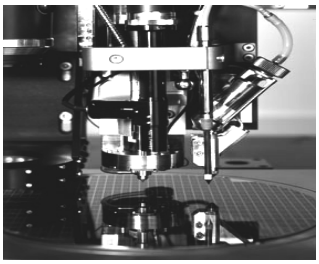


Figure 12. a. Schematic diagram of the solder jet bumping tool, and b. picture of actual tool dispensing a solder bump on a wafer using a 30 msec laser pulse width and 32 amps of laser power (PacTech SB^2 solder jetting tool).

The second bumping method which was used in this study, placed all the solder spheres at once onto the wafer using a solder sphere transfer technology. This technique is more relevant for higher volume applications where cost and throughput are critical. The basic principle of this technology is to simultaneously pick up preformed solder spheres using a patterned vacuum plate and then accurately place them onto the bond pads of the wafer.

This technique requires a tacky flux to be applied to the wafer prior to bumping. This flux acts both as a medium to hold the solder spheres in place until it is moved over to a reflow station, but also as a wetting agent for the solder. This flux is selected to be very benign, or damage would occur to the GaAs surfaces.

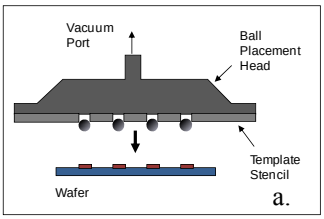
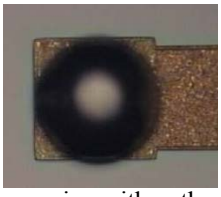


Figure 13. a. Schematic diagram of the solder sphere placement bumping tool, and b. Picture of actual tool placing solder spheres onto a wafer (PacTech Ultra-SB^2 solder sphere placement tool).

In both solder bumping techniques, the solder spheres were reflowed a second time in a vapor phase oven using formic acid or forming gas as the reducing agent (205 ºC peak temperature and dwell time of 32 secs).



Steps B9-B10: Solder bump and reflow using either the laser based sphere jetting system or the solder sphere placement system (ATV reflow oven).

The solder bumping process is typically characterized for quality by measuring the height uniformity across the wafer and by measuring the adhesion to the Ni/Au UBM [17].

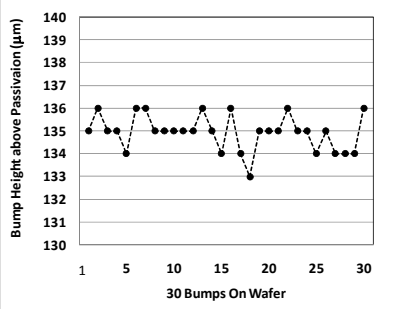
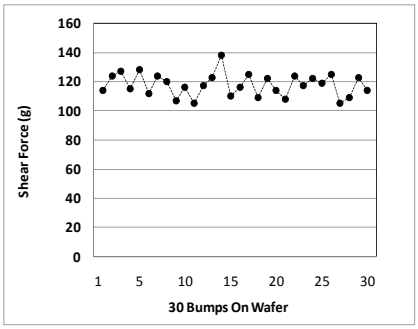


Figure 14. Plot of solder bump height on 30 pad locations across the wafer (Nikon Z-Axis measurement tool).



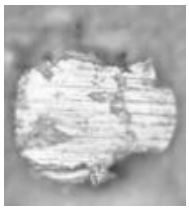
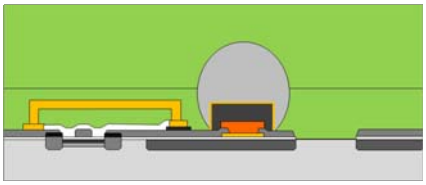


Figure 15. Plot of shear force on 30 pad locations across the wafer, bumped with SnPb Eutectic solder bumps (Dage 2400 shear tool) and image of a sheared solder bump.

The bump height uniformity for these two solder bumping technologies is expected to mimic the uniformity of the preformed sphere. Typical size specification from most solder sphere vendors is ±5µm for most flip chip sized spheres. The measured shear force gives a good indication of the adhesion of the solder to the UBM. In addition, characterization of the shear mode will give some information on the thickness and quality of the intermetallic formed between the solder and the UBM. In all cases for this study the shear mode was observed to be ductile failure in the solder.

Wafer Thinning

After bumping, many device designs require the wafer to be thinned before singulation [18]. The grinding process in inherently mechanical in nature and special care must be used to protect the frontside of the wafer. In this study, a spin on resist was deposited onto the front surface of the wafer, followed by lamination of a UV release tape on top of the resist. Several additional studies indicate that the spin-on resist step can be eliminated if special laminate films are used which are compliant and do not damage the air bridges.



Steps C11-C12: Spin on blanket layer of resist on to the frontside of wafer and then laminate a UV release film on top of the resist (Suss MicroTech MA200 spin coater and Ultron film laminator).

The wafers were then ground using a standard grinding system equipped with a Polygrind™ option. The specification for this process were a target thickness = 300 µm, target range of ± 12.5 µm, and a TTV < 10 µm.

Step C13: Grind and polish wafer (Disco DGF850 wafer grinder tool equipped with Polygrind™ option).

Table 2. Parameters used for GaAs wafer thinning.

	Course Grind	Final Polish
Mesh / Grit	20-30 µm / #600	2-4 µm / #4000
Table Speed	100 rpm	100 rpm
Removal Rate	3.89 µm/sec	0.17 µm/sec

One measure of thinning quality is the ability to repeatedly grind wafers to the same thickness. The following chart shows the thickness distribution of 600 µm GaAs wafers which were ground to the target thickness of 300 µm.

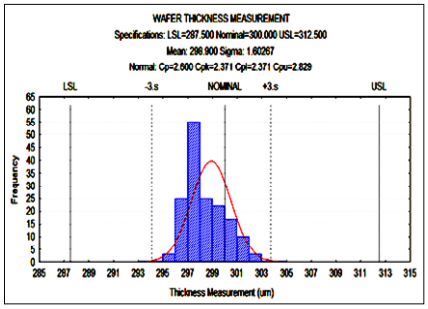


Figure 16. Chart showing the thickness distribution of wafers ground and polished (Disco DGF850).

The backside finish quality has a number of ramifications to the stability of the device through the many subsequent handling steps as well as its reliability during electrical operation. Any significant flaws or chipping can create initiation points for cracking and die breakage. A surface finish < 0.05 µm Ra was measured for these devices.

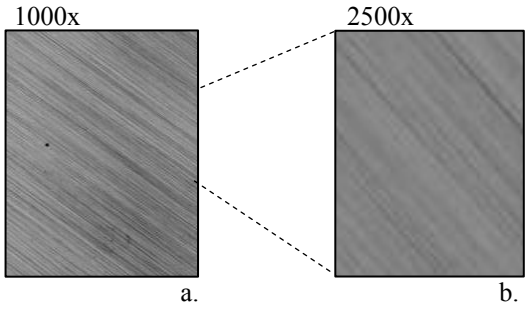


Figure 17. Optical images of a thinned GaAs wafer at: a. 1000x magnification and b. 2500x magnification (Olympus microscope).

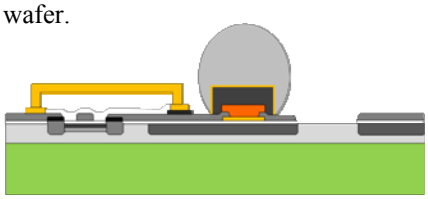
After thinning, the laminate film is removed from the frontside of the wafer.

Step C14. Expose and remove laminate from wafer frontside (Ultron UV exposure system).

Dicing

Singulation of the wafer into individual die is usually one of the last steps performed at the wafer level. The wafer is laminated to a mounting film and then cut using a high precision saw or laser. The die are then either picked and placed directly from the dicing film onto the next layer of packaging or placed into waffle packs or pocketed tape.

The wafer is first laminated to a laminate film (dicing tape on a rigid ring). The spin-on resist which is still on the frontside is then removed using a solvent while spinning the wafer.



Step D15-D16: Laminate dicing tape onto backside (Ultron laminator) and strip resist layer from front of wafer.

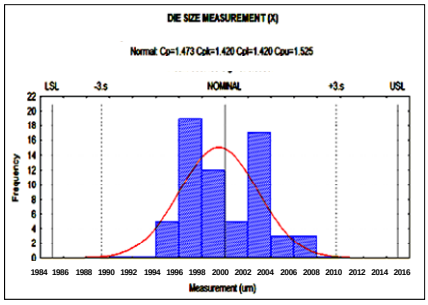
Dicing is performed using a dual spindle tool and two different blade widths.

Table 3. Parameters used for GaAs wafer dicing.

	Blade 1	Blade 2
Blade Width	35-40 µm	25-30 µm
Grit	#3000	#2000
Feed Speed	2.5 mm/sec	2.5 mm/sec
Spindle Speed	40,000 rpm	40,000 rpm

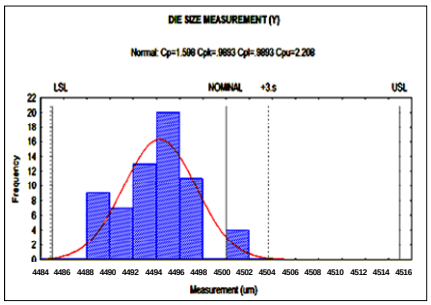
Step D17: Dice wafer using two-step cut (Disco DFD651 dicing tool).

One measure of the dicing quality is the ability to repeatedly dice the die to the same size. The following charts show the die size distribution where the target die size was 2000 µm x 4500 µm, with a tolerance spec of ±20µm.



X

Figure 18. Chart showing the die size distribution of wafer in the x direction (Disco DFD651).



Y

Figure 19. Chart showing the die size distribution of wafer in the y direction (Disco DFD651).

Another measure of dicing quality is the amount of chip-out and cracks which are observed on both the frontside and backside of the wafer.

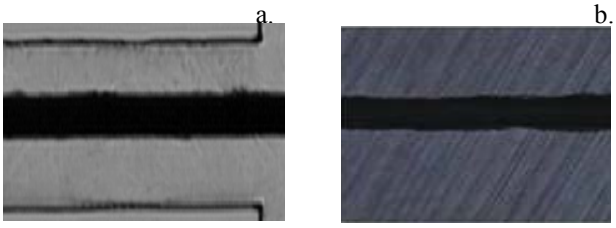


Figure 20. Optical images of the dicing quality on the a. front and b. backside of the GaAs wafer (Olympus microscope).

CONCLUSIONS

A set of packaging and backend operations were developed to process GaAs wafers: UBM deposition, solder bumping, wafer thinning, and dicing. The strategy of using a set of spin-on resists and laminate films to protect the wafer from both chemical and mechanical damage enabled the use of several common technologies to process the wafers. These processes should be applicable to other compound semiconductor devices and also wafers with special properties like MEMS, optoelectronics, and biosensors.

Future work on this program includes the processing of much larger wafer volumes through the complete process flow. This will allow benchmarking of tool time, throughput, and the labor required for each step. This will help identify any bottle necks in the process and in turn allow one to estimation of the costs for each step.

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