Silicon Interposers enable high performance capacitors

Interposers between ICs and package substrates that contain thin film capacitors have been used previously in order to improve circuit performance. However, with the interconnect inductance due to wire bonds being high, the benefits of thin film capacitors have not been fully realized. Replacing the wire bonds with Through Silicon Vias (TSVs) in the interposers with capacitors provide the shortest electrical path between devices and the decoupling capacitors**.** TSVs with their very low inductance will enable higher electrical performance when integrated with embedded thin film capacitors.

ALLVIA has conducted studies of various capacitors on silicon interposers. The data presented in this paper shows that after 1000 thermal cycles planar capacitors on silicon result in stable, reliable devices operating at higher frequencies than discrete devices.

The Case for Silicon Interposers – 2.5D Packaging

The increasing demand to exchange massive volumes of electronic data has caused chip speed capabilities to outstrip chip package capabilities at a rate greater than ever experienced by the electronics industry.

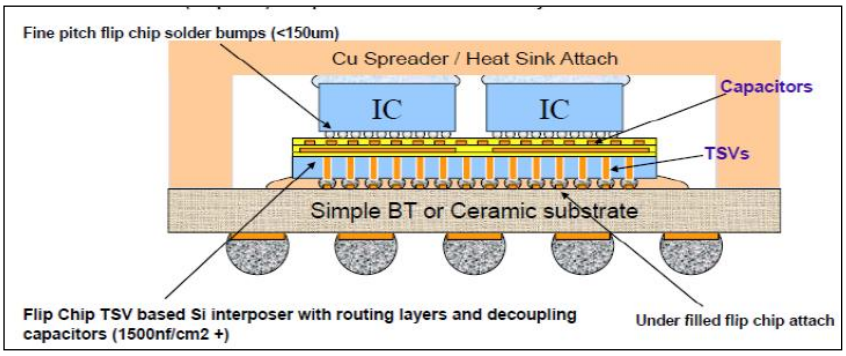

Figure 1 – Stacked die on interposer and stacked plus adjacent die on interposer

For years the semiconductor packaging industry has explored the use of multi-chip approaches to provide alternative packaging solutions for these needs. However, the higher cost and lower yields of these approaches, especially for the mature horizontally mounted multi-chip, or MCM of the early 1990s proved to be unacceptable for large volume needs.

Now the industry is exploring vertical methods for creating multi-chip modules and a chip-to-chip interconnection method enabling higher performance interconnection that promises to transcend the issues that stunted MCMs.

Silicon Interposers provide an economical and higher I/O density platform than resin substrates to hold and interconnect an array of chips. Chips can be mounted either vertically or in a combination of horizontally and vertically (shown in Figure 1). In addition to providing electrical interconnection and mechanical support the interposer with TSVs can also provide heat transfer. Using conventional redistribution metal layers (RDL) an interposer enables the finer pitch interconnections of the IC chips to be fanned out, or interposed to larger pitches for economical assembly to a traditional IC package substrate, such as a BGA.

Unlike wire bonds and large solder balls, newer interconnect methods, such as micro bumps or copper pillars, can be mounted to interposers using assembly processes that enable rework and repair if needed.

The importance of Capacitor positioning to achieve electrical performance

Optimum capacitor position is essential to achieve adequate chip protection from signal interference. Optimum position means that the capacitors must be placed as close as possible to the ICs needing protection from interfering signals in order to minimize the effect of trace and via inductance.

Figure 2 shows the high frequency model of a bypass capacitor with trace inductance.

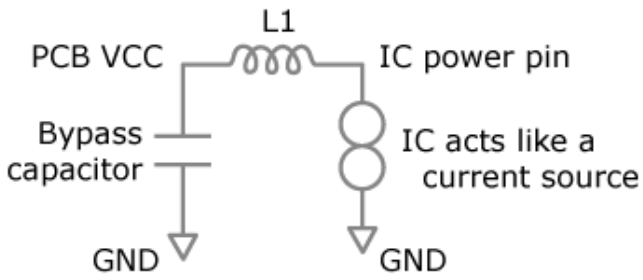

Figure 2 IC with bypass capacitor circuit model

Figure 3 illustrates the impedance versus frequency response of a typical surface mount chip capacitor. To the left of the Self-Resonance point (SR) the device impedance will be capacitive. At frequencies above the self-resonance point the device is inductive. This means the capacitor will shunt and protect the IC in the capacitive frequency range. However, above the SR point the device offers no protection.

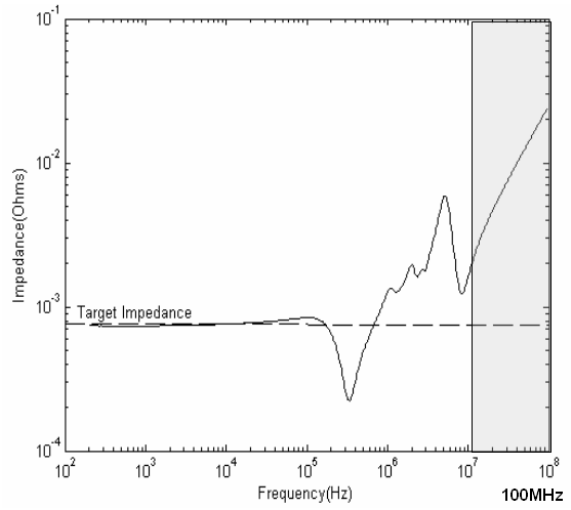

Figure 3 Impedance versus frequency response of a typical surface mount chip capacitor. Source: "Design, Modeling and Characterization of Embedded Capacitors for Decoupling Applications." Muthana et al

One consequence of traces with vias connecting capacitors is self and mutual inductance. The effect of these inductances is to lower the SR point reducing the range of frequency over which the capacitor will provide protection.

Using any of the available modeling tools, a designer would quickly conclude that separating a decoupling capacitor from the chip by any length of trace and vias will add detrimental inductance and lower the effectiveness of the capacitor.

Optimum placement of the capacitors needs to minimize inductance and resistance. The benefit of adding capacitors to the interposer is to minimize the effects of trace and via self-inductance.

The merits of thick and thin film capacitors on Interposers

Fabricating planar plate capacitors on silicon interposers is a fairly straightforward process. The choice of the dielectric is possibly one of the most challenging aspects. Thin film dielectrics offer very high capacitive values in small areas. ALLVIA currently is capable of producing capacitors with values up to 1500 nfd/cm^2. A 2500 nfd/cm^2 capable process is in development (as of Q1 2011) and has passed a 1000 cycle reliability test.

Using different dielectric thicknesses and plate areas enables other capacitor values to be reliability produced..

In contrast thick film dielectrics, such as silicon dioxide offer capacitance values in the ranges of 20 to 80 nfd/cm^2.

Thick film dielectrics generally offer lower cost, higher breakdown voltages, and lower leakage currents than thin film. However, thin films offer higher capacitance per unit area.

ALLVIA offers both thick and thin film dielectric choices.

Using TSV interconnections to achieve optimum performance

Thin film capacitors without TSVs have been used previously. However, with the inductance of the interconnecting wire bonds and RDL layers being high, the benefits of thin film capacitors have not been fully realized. TSV interposers with embedded capacitors provide the shortest electrical path between devices and power supply decoupling capacitors. TSVs with their very low inductance enable higher electrical performance when integrated with embedded thin film capacitors.

ByPass Capacitor Comparison

Bypass capacitors tend to require large capacitance values. Figure 4 shows the comparison of 15 nFd capacitors – one being a 0402 sized, XR7 grade ceramic chip capacitor and the other a thin film planar capacitor on a silicon substrate.

The physical area of the capacitors is very close – 1000um x 500um for the 0402 chip and 950 x 950 um for the planar thin film capacitor. The height of the thin film cap is substantially less than the thick film cap.

As shown in figure 4 the thick film chip cap has an SR ≈ 55 MHz and the planar thin film cap has a significantly higher SR ≈ 175 MHz.

Much of this increase in SR can be attributed to the reduction in capacitor inductance. The chip cap is approximately L_c chip ≈ 0.7 nH* and the planar is L_c planar ≈ 0.07 nH

Part #	C (nfd)	L (ph)	R (mOhms)	Resonant Freq (Mhz)
Thin Film w TSV	14.8	66	104	175
X7R	15.0	710	128	55

Source:
http://www.kemet.com/kemet/web/homepage/kfbk3.nsf/vaFeedbackFAQ/D1A54E16FEC61B058525721E006EF53C/$file/Sun%20Paper%20on%20ESL%20&%20ESR.pdf

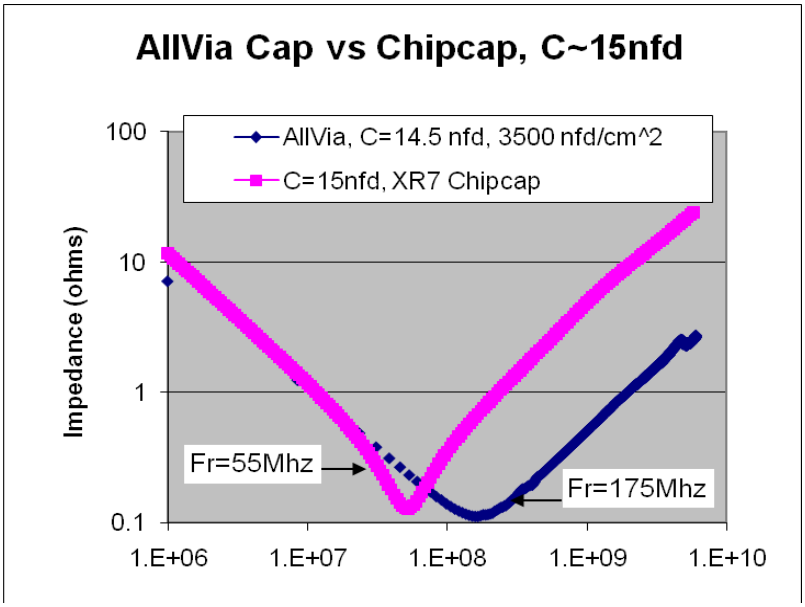

Figure 4 Comparison of the SR (F_r) of an 0402 ceramic chip cap and a planar thin film cap.

Test and Reliability Results

Testing of Interposers and Capacitors on Interposers includes standard electrical tests of capacitance and resistance at low frequencies and capacitance tests at high frequency.

The wafer level reliability testing conducted by ALLVIA includes interposers with TSVs and planar capacitors. Package level reliability testing is done with capacitors on interposers with bumped TSVs on BT substrates. The packages have underfill epoxy between the interposer and the BGA substrate and are bumped with a lead-free solder. The standard reliability test is thermal cycling done to JEDEC condition "B" –55 to 125 deg C, two cycles per hour.

For all reliability tests there is a 0 time pre-screening done on the samples to be tested. Readouts are done at 250 cycles, 500 cycles, 750 cycles, and 1000 cycles.

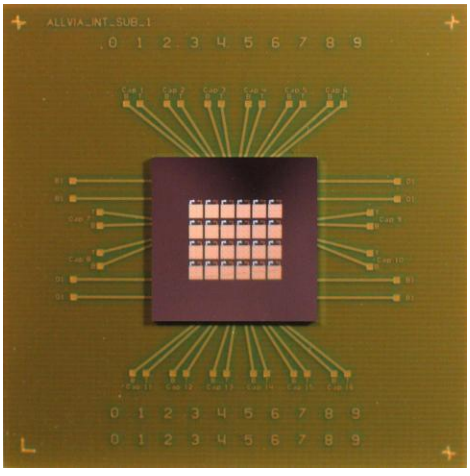

Figure 5 Photo of one of AllVia's Capacitor on Interposer with TSV soldered onto a BT substrate.

Backside TSV Wafer Level Reliability Test

- 80um via diameter 200um deep
- Long daisy chain vias plus interconnects

Wafer ID	0 cycles		500 cycles		1000 cycles		
	R avg mOhms	Std Dev mOhms	R avg mOhms	Std Dev mOhms	R avg mOhms	Std Dev mOhms	Failures %
J12-SWB5	26.5	13	21.5	6.5	23	6	0
J12-SWF3	31.5	7	25.5	3.5	22	5.5	0

Capacitor Wafer Level Reliability Test (Wafer ID 341-F1)

- Two types of capacitors were measured; standard and high capacitance
- 51 devices for each type of capacitor
- 20 devices assigned for Breakdown Voltage

	0 cycles	250 cycles	500 cycles	1000 cycles
Standard Caps (1Mhz)	457 nfd/cm^2	466 nfd/cm^2	457 nfd/cm^2	446 nfd/cm^2
Breakdown Voltage (avg)	8.9 v			8.7 v
High Capacitance Caps (1Mhz)	2506 nfd/cm^2	2281 nfd/cm^2	2217 nfd/cm^2	2130 nfd/cm^2
Breakdown Voltage (avg)	7.7 v			8.7 v

TSV Package Reliability Test

- Daisy chain through filled Cu Vias, bumps, and organic substrate with underfill.
- Resistance includes routing on interposer, chain of 8 vias, lead-free solder bumps, and routing on BT substrate.
- Failure criteria: resistance change from starting resistance > 3 sigma of the measurements.

Number of Cycles	0 cycles		250 cycles		500 cycles		750 cycles		1000 cycles	
	Average Resistance (Ohms)	Std Dev (Ohms)	Average Resistance (Ohms)	Avg % change (Ohms)	Average Resistance (Ohms)	Avg % change (Ohms)	Average Resistance (Ohms)	Avg % change (Ohms)	Average Resistance (Ohms)	Avg % change (Ohms)
Resistance	5.72	0.21	5.70	-0.41%	5.76	0.68%	5.79	1.22%	5.81	1.57%
# of new failures	2/120 (Time Zero)		0/118		0/118		0/118		0/118	

High Frequency Capacitance Measurements

Small value bypass capacitors with different values can be used together for impedance frequency shaping. Smaller value capacitors may be used for non-bypass applications and offer even higher effective operating frequencies.

Below and graphed in Figure 6 are the results of a sample of 0.304 nfd and 14.8 nfd capacitors tested over a range of 1 MHz to 6 GHz. The SR point is approximately 1.4 GHz and 175 Mhz respectively.

- Measurements done from 1Mhz to 6 Ghz at the wafer level
- Both thick dielectric and high capacitance capacitors measured.
- 25 devices measured on each wafer.
- Thick film capacitor: C1 = 0.304 nfd, L=39 pfd, R= 44 mOhms*, Fr = 1.4Ghz.
- Thin film (high capacitance) capacitor: C2= 14.8 nfd, L=66 pfd, R= 104 mOhms*, Fr= 175 Mhz.

*The resistance (or ESR) for the devices was extrapolated from the data measurements.

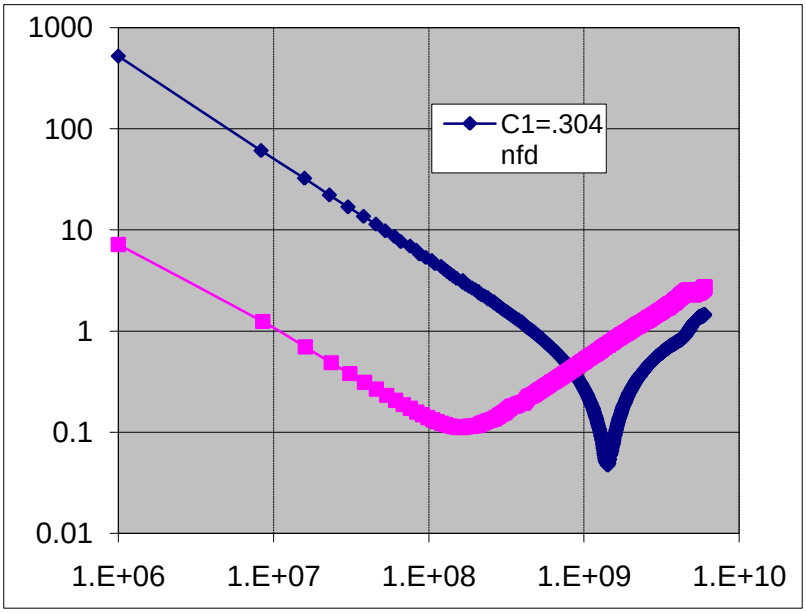

Figure 7 The results of a sample of 0.304 nfd and 14.8 nfd capacitors tested over a range of 1 MHz to 6 GHz

Summary

Silicon interposers with both embedded capacitors and through silicon vias for interconnection offer chip designers a new means to achieve high speed and high frequency performance.

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