Copper Pillar & Micro Bump Inspection Requirements and Challenges

Rudolph Technologies, Inc.

A 3D/2D APPROACH TO INSPECTION

Miniaturization has been one of the main driving factors in devising new technologies and new innovations since the advent of the semiconductor industry. This, along with packing more power in each chip has been the challenge that designers have faced and are facing to this day.

The advent of flipchip wafers was an important step towards this seemingly never-ending challenge. This technology allowed chip designers to increase number of I/Os by distributing them over the entire surface of the die as compared to the wire bond technology which only used its periphery. The use of the entire die surface allowed designers to decrease the size of the die and at the same time to increase its functionality. The original flipchip technology was pioneered by IBM and Delco over 40 years ago. IBM's C4 technology used an evaporation method to deposit solder on die surface producing typically 200-250µm spherical bumps. Over the years, not only have cheaper and faster bumping technologies been devised, but they have been subject to the same miniaturization as the rest of the semiconductor industry. Bump height, bump diameter and pitch have been shrinking ever since. Micro bumps are one of the latest developments in bump technology to follow the miniaturization path. As its name suggests, these bumps are the smallest that today's technology offers.

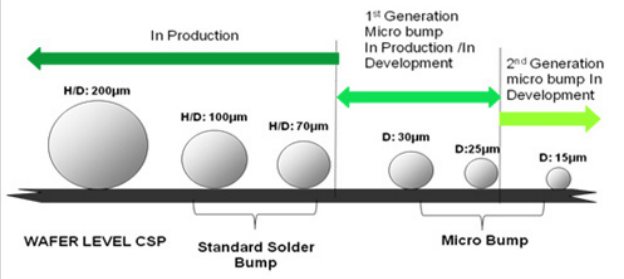


***Figure 1** - Shows the different bump sizes currently in production and in development*

Although dimensions of the first generation micro bumps could somewhat vary, typical bump sizes currently in production are about 25µm in diameter and 50µm in pitch. In addition, some companies are developing the next generation micro bumps with sizes as small as 15µm in diameter but they are not expected to be in production until 2010.

As mentioned earlier, a typical application for micro bumps occurs when an unusually high number of I/Os are required or the overall size of the die is extremely small. A Through-silicon Via (TSV) package is one example of such case, requiring a high number of I/Os within a die. Today there are dies in production with as many as 25,000 bumps per die. It is expected that this number will increase to 50-60,000 per die in the next year or two.

PILLAR BUMPS

Another form of bump gaining more popularity is the pillar bump. These bumps, instead of being spherical in shape, are in the form of a pillar, with various shapes and sizes. The most popular shape is in the form of a cylinder. The pillar shape allows the high ratio of bump height to bump diameter, therefore allowing very tight pitch even when bump heights are large. Sometimes a solder cap is formed on top of the pillar to help with connectivity with the mating chip (Fig. 2). The ability to dissipate heat is another advantage of these bumps, making them good candidates for microprocessors.

Bump height can vary anywhere from 5µm to 100µm and diameter from 10-20 to 100µm and larger. Most pillar bumps now in production are larger than 20µm in height.

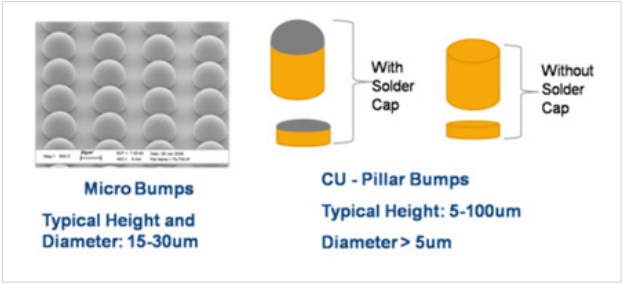


Figure 2

TYPICAL INSPECTION REQUIREMENTS

Although micro bumps and pillar bumps have different shapes and a somewhat different manufacturing process, the inspection requirements are very similar. The requirements can be broken down in two different categories, bump metrology and bump defect, as illustrated in Figs. 3 and 4.

1. Bump Metrology – 3D and 2D
   a. Bump Height – 3D
   b. Bump Coplanarity – 3D
   c. Bump Diameter – 2D
   d. Bump position – 2D

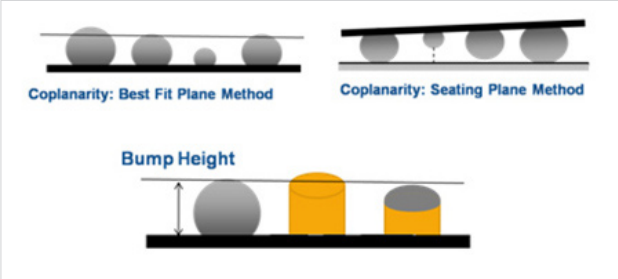


Figure 3

1. Bump Defect – 2D
   a. Missing bump
   b. Bridge bump

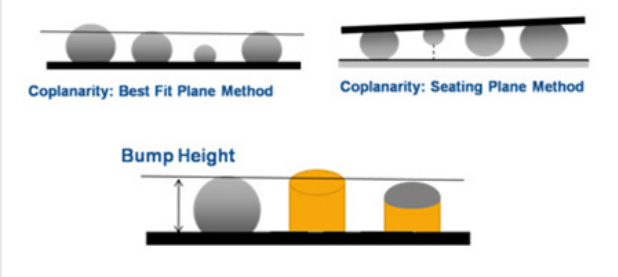


Figure 3

Figure 4

INSPECTION CHALLENGES

Two main factors contribute to the challenges facing inspection of micro solder bumps and/or copper pillar bumps: their relatively small size and the large number of bumps often found in one die.

Typical micro bumps in production today have diameter of >20µm. Even now, bumps as small as 15µm in diameter are being developed for the next generation interconnects. Cu Pillar bumps, on the other hand, have a wide variety of sizes. Their diameter can range anywhere from 20µm in diameter and larger with height as small as 5µm. As their micro solder bump relatives, bumps as small as 10µm in diameter and smaller are being developed today in R&D labs.

As micro solder and pillar bumps become smaller, so do their manufacturing tolerances. For example, the height of a 100µm bump can have a tolerance of ±10µm, whereas the acceptable height variance of a 25µm bump could be ±1µm. This means that an inspection system inspecting micro bumps must have higher performance capability as compared to systems inspecting larger bumps. To be more exact, the rule of thumb for an acceptable inspection performance is that its repeatability and reproducibility performance be within 10% of the total tolerance band. Considering this rule, a system inspecting 100µm bumps need only have repeatability of 2 µm at 3σ but a system inspecting 25µm bumps has to perform at 0.2µm, 3σ repeatability.

Different inspection technologies can offer performances far above what is typically needed for bumps today. However, the challenge is to use a technology that can combine acceptable system performance without completely sacrificing throughput. This is an extremely important factor for a system used for production purposes. The faster the throughput, the lower the cost of inspection per die.

Another challenge facing the inspection of micro bumps is the typically high number of I/Os per die. Dies are now being produced with greater than 20,000 bump/die with roadmaps showing an increase to >50,000 per die. These numbers challenge the computing and processing speeds at which bump dimensions can be inspected, and can affect total throughput.

The challenge is to select an inspection technology that enables precise and repeatable performance while maintaining superior throughput.

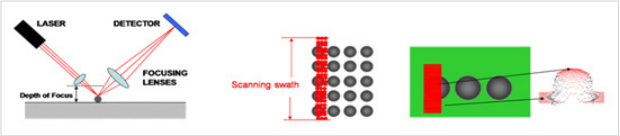


Figure 5

Unlike some technologies, the number of bumps on the wafer has minimal affect on the throughput since the entire wafer is scanned anyway. This is a major advantage of this technology to make it suitable for use in production.

INSPECTION USING 2D CAMERA

Even though laser technology uses a powerful sensor to inspect 3D bump features, it has limitations inspecting 2D features of the bump, including defects such as missing bumps and bridge bumps. Furthermore, inspecting for defects on the surface of the wafer is a common process requirement. 2D cameras (TDI line scan or CCD), along with appropriate bright field/dark field lighting are the ideal method for these inspection requirements. This combination can provide both the required resolution, by selecting the appropriate microscope lens, and the high throughputs needed for 100% inspection of wafers.

Two test cases examine inspection performance using laser technology are discussed below:

Case 1: A micro solder bump wafer is inspected for 3D and 2D bump metrology. Each bump has a diameter of 20µm and height of 22µm. The entire wafer is scanned and 3D data points are collected on the bump top and wafer surface. A contour plot of the 3D data points over the wafer surface is shown in Fig. 6.

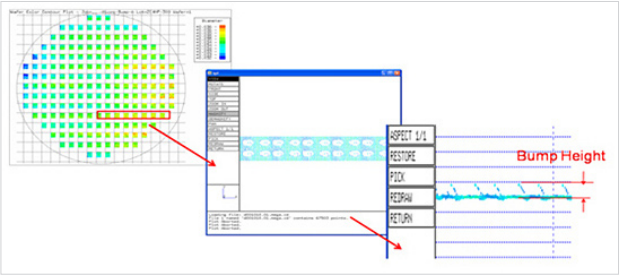
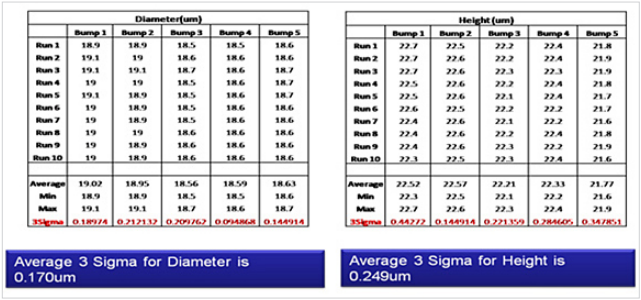


Figure 6

To measure the repeatability performance, five bumps were randomly selected, each bump diameter and height were measured ten times. Table 1 shows the repeatability performance achieved.



Diameter(um)

	Bump 1	Bump 2	Bump 3	Bump 4	Bump 5
Run 1	18.9	18.9	18.5	18.5	18.6
Run 2	19.1	19	18.6	18.6	18.6
Run 3	19.1	19.1	18.7	18.6	18.7
Run 4	19	19	18.5	18.6	18.7
Run 5	19.1	18.9	18.5	18.6	18.7
Run 6	19	18.9	18.5	18.6	18.6
Run 7	19	18.9	18.5	18.6	18.6
Run 8	19	19	18.6	18.6	18.6
Run 9	19	18.9	18.6	18.6	18.6
Run 10	19	18.9	18.6	18.6	18.6
Average	19.02	18.95	18.56	18.59	18.63
Min	18.9	18.9	18.5	18.5	18.6
Max	19.1	19.1	18.7	18.6	18.7
3Sigma	0.18974	0.212132	0.209762	0.094868	0.144914

Height (um)

	Bump 1	Bump 2	Bump 3	Bump 4	Bump 5
Run 1	22.7	22.5	22.2	22.4	21.8
Run 2	22.7	22.6	22.2	22.4	21.9
Run 3	22.7	22.6	22.3	22.3	21.9
Run 4	22.5	22.6	22.2	22.4	21.8
Run 5	22.5	22.6	22.1	22.4	21.7
Run 6	22.6	22.5	22.2	22.2	21.7
Run 7	22.4	22.6	22.1	22.2	21.6
Run 8	22.4	22.6	22.2	22.4	21.8
Run 9	22.4	22.6	22.3	22.2	21.9
Run 10	22.3	22.5	22.3	22.4	21.6
Average	22.52	22.57	22.21	22.33	21.77
Min	22.3	22.5	22.1	22.2	21.6
Max	22.7	22.6	22.3	22.4	21.9
3Sigma	0.44272	0.144914	0.221359	0.284605	0.347851

Average 3 Sigma for Diameter is 0.170um

Average 3 Sigma for Height is 0.249um

Table 1

Case 2: A wafer with 20 µm diameter, 5 µm height Cu pillar bumps was inspected for height and diameter. The contour plots in Fig. 7 show inspection capabilities of the laser technology and repeatabilities achieved over the entire wafer.

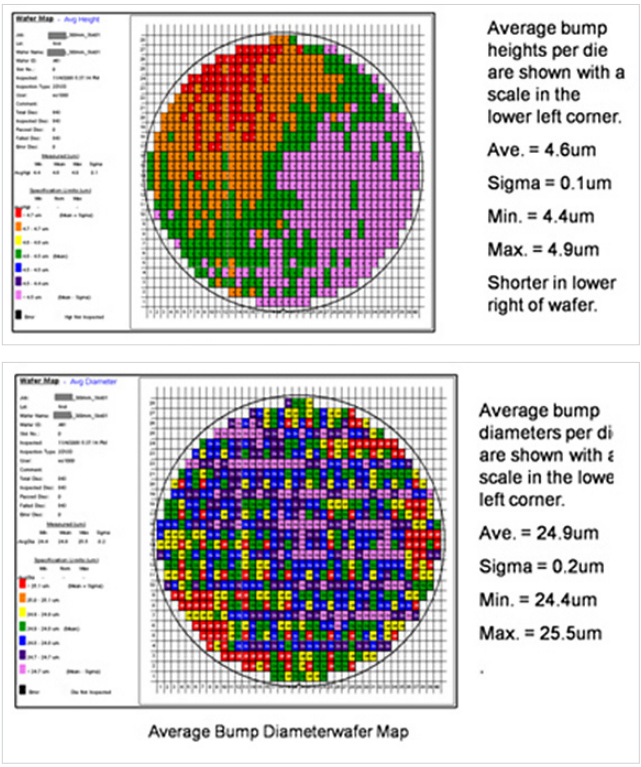


Figure 7

CONCLUSION

Line scan laser technology provides sufficient resolution to inspect micro bumps and Cu pillar bumps while delivering acceptable repeatability performance. Furthermore, this technology enables precise measurement performance and excellent throughput, making it ideal for today's high-volume production environment. Laser technology also allows for the inspection of larger standard bumps, providing flexibility for the inspection system. Finally, a laser sensor can be coupled with a 2D camera to provide inspection capability, not only for 3D but 2D metrology and surface defects.