

CHARACTERIZING TRANSFER EFFICIENCIES AND THE FINE FEATURE STENCIL PRINTING PROCESS

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ABSTRACT

Electronic device footprints continue to shrink, requiring smaller and smaller solder deposits to be consistently produced during the stencil printing process. The transition to lead-free assembly also creates tighter process windows, due to the alloys' lower spread characteristics. This situation represents a dual challenge for assemblers: not only is development work required to meet miniaturization trends; more is required to understand the behavior of lead-free solder materials.

Stencil printing research over the past four years has aided in demystifying the printing process by understanding the influence of the stencil manufacturing process, providing models to predict actual volumes of fine features, improving stencil-PWB alignment, maintaining stencil aperture libraries, and maximizing lead-free cosmetics and yields. The most recent research has been focused on improving fine feature prints on boards that require thick stencils and modeling transfer efficiencies of modern pastes.

KEYWORDS: Stencil printing, transfer efficiency, fine features, aperture design, MicroStep pockets, lead-free

INTRODUCTION

The basic goal of stencil printing is to deposit the proper amount of solder paste in the proper location. Although this appears to be a simple goal, many factors influence the process. These factors are well known, but not always easy to control.

Even when the best way to robustly deposit the proper amount of paste is known, it may not be possible. PWB designs often combine fine feature devices which require thinner stencils with through-hole connectors or RF shields which require thicker stencils. This leaves a dilemma for the assembler: how to accommodate both requirements to ensure the proper amount of paste for each device. The study described in this paper focuses on how to get the best print quality for fine feature devices when working with a variety of stencil

thicknesses, with both tin-lead and lead-free solder pastes. It also seeks to define transfer efficiency models for modern, current-generation solder pastes.

Research Review

Research on the how the stencil itself influences the stencil printing process began in 2001 with a print optimization study.¹ This study, which evaluated the effects of stencil design and fabrication processes on print performance, provided the basic understanding and foundation for future research. The study examined the effect of aperture size, shape, degree of taper and electropolish on solder paste release. Release was measured as transfer efficiency, which is calculated as the volume of paste actually deposited divided by the volume of the stencil aperture, and expressed as a percent.

This study quantified the mechanics of stencil release by using a specially designed and calibrated stencil. A single type 3, no-clean solder paste was used. To eliminate the noise caused by circuit board variation, print tests were performed on solder mask covered copper substrate material. The subsequent analysis of over 10,000,000 data points revealed excellent information about manufacturing techniques, but the most amazing result was the high dependence of transfer efficiency on the area ratio of the stencil aperture itself.

Area ratio is defined as the area of the circuit-side opening of the stencil divided by the area of the aperture walls. This is important because solder paste adheres to any surface it contacts, and the surface tension holding the paste to the circuit pads must overcome the surface tension holding the paste to the aperture walls in order for the paste to release.

For area ratios less than 0.7 (square or circular apertures of 14 mils or less in a 5 mil thick foil) transfer efficiency was modeled as follows:

$$TE = 100 \times (2.535 \times AR^{3.426})$$

where

TE represents Transfer Efficiency

AR represents area ratio

The relationship can be viewed graphically in Figure 1.

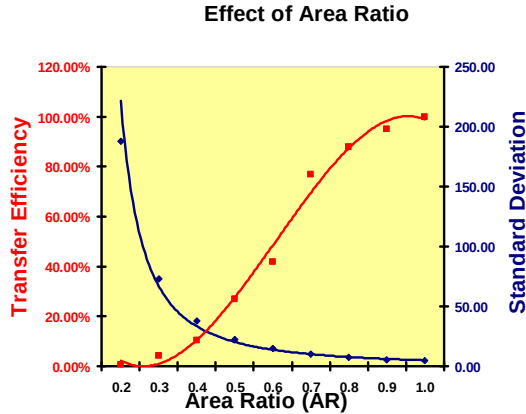


Figure 1. Plot of transfer efficiency vs. area ratio, including standard deviation. Notice the linear relationship in the 0.5 to 0.7 range, which encompasses feature sizes from 10 to 14 mils on 5 mil foil.

The statistical analysis of the study that produced this model showed that for a given solder paste and print parameters, 95% of the transfer efficiency is dependent on area ratio. Other factors such as degree of taper, electropolish, and experimental error contributed 5% to the transfer efficiency of paste. It was also found that as the area ratio increased, the standard deviation of transfer efficiency decreased, giving more repeatable print volumes.

A solder paste volume predictor model was developed from the data that was generated, and was used extensively to aid in stencil design when fine feature devices were involved. In many cases larger, more repeatable volumes could be achieved with thinner foils. In earlier applications, the design of the circuit board permitted thinner foils, as small BGA-type devices were typically used with other miniaturized components. But the proliferation of these devices now puts them on circuit boards which also have demands for high volumes of solder paste, e.g. intrusive reflow, heat sink attachment, or RF shields. Stencil design now becomes a difficult balancing act.

A new experiment was designed to build upon the original work. In the years since the study, improvements in solder paste formulations have improved fine feature print capability, and the enhanced performance of the newer formulations require new models to be generated. A new stencil design option was also introduced, which also requires characterization.

The following project studies the transfer efficiency of solder pastes using stepped stencils with 0.5mm area array

devices. It looks at the effect of straight (naturally tapered) walls, stepped-down areas around devices, and microstep pockets. All print data was taken on actual PWB's with the intention of introducing the normal variation caused by solder mask, traces, board support, printer alignment capability, and other variables intrinsic to SMT printing. Figure 2 illustrates the three aperture profiles.

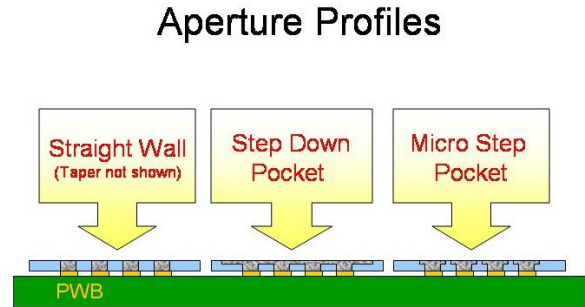


Figure 2. Profiles of three types of aperture designs: traditional, straight walls with a slight taper that results from the laser cutting process; traditional stepped down areas that are typically used to improve fine feature printing, and the new MicroStep pocket.

A MicroStep pocket is an individual step down around each aperture and concentric with it. It is formed in a chemical etch process similar to regular step downs, but must be registered very precisely. Initial applications of the microstep were successful increasing deposit size in some very tight areas (<10 mil) on thick foils (5 and 6 mil). In these initial applications, volume data was not available from the assembler, but visual assessment of the prints showed larger paste deposits with the microstep. Figure 3 illustrates a close up cross section of the aperture.

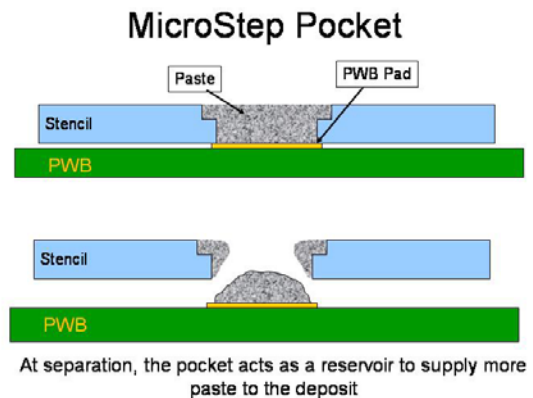


Figure 3. Illustration of MicroStep Pocket. Notice the stepped down area does not span the entire device; instead it steps down for each individual aperture. This makes stepping stencils possible when direct pressure print heads are used.

It should be noted that Figure 3 is a schematic diagram for reference purposes only. The actual cross section of a microstep pocket would show natural rounding at the corners, which is a characteristic of the chemical milling process that produces them.

A traditional step down in a stencil is often limited by the clearance area around the device. If enough clearance is not possible due to layout density, fill pressure of the squeegee can be compromised at the perimeter of the device. If the assembler uses enclosed print head systems, stepping the top side of the stencil is not possible because it can cause damage to the blades. The microstep pocket provides a solution to both adverse situations. Because each aperture is stepped individually, clearance around the device is no longer a factor in stencil design. And because the squeegee side of the stencil appears to have regular aperture opening with no step around the perimeter, enclosed print heads are not affected.

EXPERIMENTAL METHOD

Materials

To measure the effects of the three stencil designs, a small experiment was designed using two fine feature devices, two solder pastes, and three aperture profiles. The devices were 0.5 mm pitch uCSP98 and CABGA56. The CSP package used nominal pad sizes and board-side aperture openings of 10 mils. The CABGA 56 used nominal pad sizes and board-side aperture openings 12 mils. The boards were screened to ensure pad sizes were correct. The stencils were measured for actual squeegee-side and board-side aperture openings and foil thicknesses. These measurements were used to calculate the actual volumes of each aperture, which were subsequently used in the transfer efficiency calculations.

Recommended no-clean type 3 tin-lead and lead-free solder pastes were used. The tin-lead product was OM-5100 Sn63 and the lead-free was OM-338 SAC 305 alloy. It is widely understood that the metallurgy of the powder itself does not affect a paste's print characteristics. The print characteristics are based on the flux and carrier formulation. But because flux formulations are based on the alloys in the powder, it is reasonable to expect performance differences between formulations. Early formulations of lead-free solder pastes did fall short of their tin-lead counterparts in printability, but modern pastes should rival their performance. The lead-free paste used in this study has been commercially available for two years.

Four stencil thicknesses were used: 3, 4, 5, and 6 mil foils, each stepped as shown in figure 4.

Stencil Design

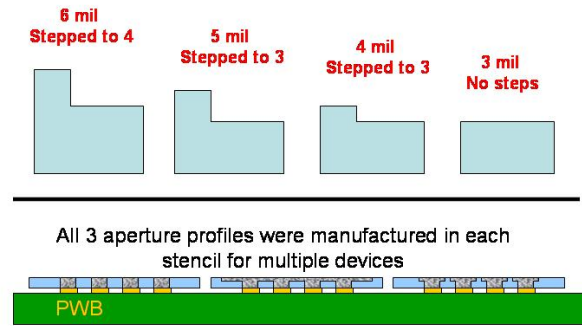


Figure 4. Stencil and step configurations used in this study.

The test vehicle used was the CERF board, which contains numerous sites for each device. Immersion silver surface finish was used due to its durability throughout repetitive cleaning cycles needed in this test. The board is shown in Figure 5.

0.5 mm Devices

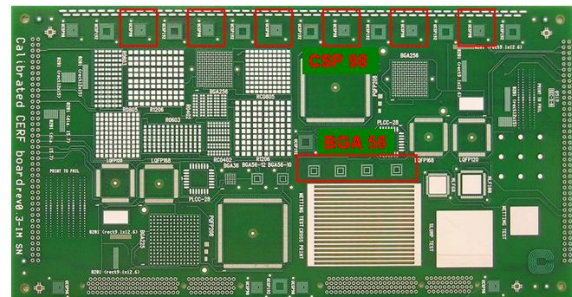


Figure 5. Test Vehicle and devices used in study

Print tests

For each paste-stencil combination, the boards used for data collection were numbered, cleaned and reprinted in sequence to limit experimental error. They were printed on an MPM Ultraflex 3000, with a print speed of 4 inches/second, a print pressure of 1.25 lbs/inch of blade length, and a separation speed of 0.5 inches/second. The first four boards were printed and discarded. Then alternate prints were used for measurement so that all data taken came from a rear-to-front squeegee stroke, again to limit experimental error. Blades were leveled after each stencil change. The stencils were manually wiped from the underside before each measured print.

To minimize alignment issues, stencils were scaled to match the circuit boards' positional accuracy. Stencil scaling is the practice of measuring the actual centroids of

devices on the fabricated PWB and applying the “actual” gerber data to the stencil file before cutting.² This practice compensates for the shrink and stretch of PWB’s that result from the fabrication process,³ and can also be used to compensate for over- or under-etch of the pads. In this experiment, the PWB’s were measured for positional accuracy and the stencil gerber was corrected. No compensations were needed for pad sizes.

Data Collection

A GSI 8200 was used to measure the volumes of the solder paste deposits. For each paste-stencil combination, data was gathered from four boards, in the locations shown in figure 5. Data was analyzed for four BGA 56 and six CSP 98 devices from each print.

The last print was visually documented with a photograph showing typical print quality of each aperture profile for each device. When removed from the printer, the stencil apertures were also photographed to document the presence or absence of paste.

It should be noted that as feature size decreases, measurement accuracy also decreases. Previous studies have shown that the measurement system used in this experiment provides good data accuracy down to 12 mil features. Measurement error is introduced at 10 mil feature sizes, but with an understanding of the limitations, one can still draw valid conclusions by examining the trends. Measurement error is considered unacceptable at 8 mil feature sizes.

RESULTS

Volumes and Repeatability

Figure 6 shows the results for BGA 56 devices with 12 mil features.

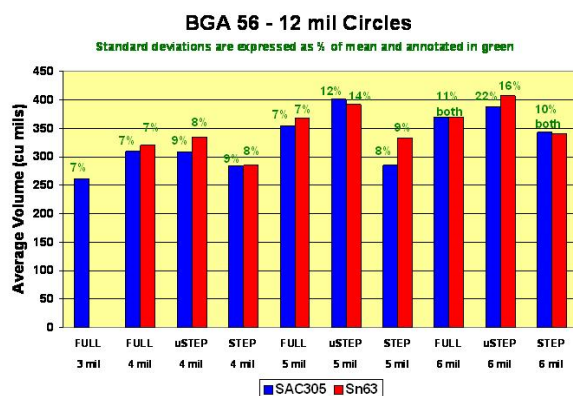


Figure 6. Average volumes and standard deviations for BGA 56 devices with 12 mil circular features. Note that all print data was generated on PWBs in a typical printing environment.

The commonly employed rule-of-thumb on print volumes of this size is that standard deviations within 10% of mean are acceptable. Applying this metric to the above data, nearly all

data points show good repeatability, for both the tin-lead and the lead-free pastes.

The data also shows that when printing 12 mil features, the most robust printing can be achieved by using straight (tapered) walls on 4, 5, and 6 mil foils. Although the microstep pockets provide slightly higher average volumes, the variability in the volumes also increases.

Figure 7 shows the results for CSP 98 devices with 10 mil features.

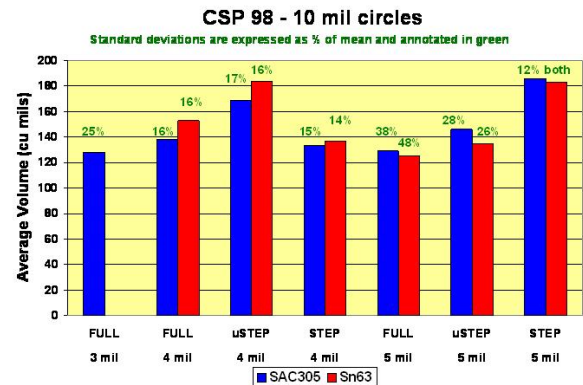


Figure 7. Average volumes and standard deviations for CSP 98 devices with 10 mil circular features. Again, note that all print data was generated on PWBs in a typical printing environment.

The commonly employed rule-of-thumb on print volumes of this size is that standard deviations within 15% of mean are acceptable. The rule is a bit looser on the 10 mil features than larger sizes because the repeatability and reproducibility of the measurement system is lower at this feature size, and more measurement error is introduced to the data. When this metric is applied to the above data, not all scenarios offer good repeatability. As expected, the challenge of printing a 10 mil feature with a 5 mil foil (Area ratio of 0.5) benefits from the use of a stepped down area. In this case, not only are average volumes higher, standard deviations are lower.

When printing 10 mil features with a 4 mil foil, no benefit was shown by stepping down the entire device area, but some benefit was shown by the use of microsteps. It is up to the assembler to determine whether the small gain in paste volume justifies the increase in stencil cost and lead time. Although the microsteps did show improvements in average volumes for area ratios of 0.45 to 0.55, in some cases they also introduced more variation, so they should be approached with care.

Although data was collected and analyzed for printing 10 mil features with a 6 mil foil, the practice is strongly discouraged, regardless of aperture profile. Standard deviations for all aperture configurations were 50% of

mean and larger, indicating a lack of robustness. This is to be expected, as the area ratio in this situation is 0.42.

Transfer Efficiency Models

The print performance of both pastes was nearly identical. Individual Student's t tests showed no statistically significant differences in their performance. Because the transfer efficiencies were equivalent, the data was grouped and analyzed together and treated as a larger sample size.

The regression model of the transfer efficiencies showed linearity in the area ratio range of 0.4 to 1.0. 0.4 was the lowest area ratio tested. It should be noted, however, that area ratios of less than 0.5 are still not recommended; recall that standard deviation increases as area ratio decreases, indicating more variability in volume consistency when small area ratios are employed. Given any particular configuration of required stencil thickness and aperture diameter, the optimum stencil design and aperture profile can be predicted using the charts in figures 6 and 7.

The equation that represents transfer efficiency for these pastes is as follows:

$$TE = \text{SQRT}(0.995 - 3.008 \cdot (1 - AR)^2)$$

where

TE represents Transfer Efficiency

AR represents area ratio

It is shown graphically in figure 8, where the blue datapoints and trendline represent the most recent tests, and the red data points and trendline represent the benchmark study in 2001. The current generation paste shows far better release characteristics throughout the entire area ratio range that was measured (0.4 to 1.0).



Figure 8. Transfer efficiency comparison of different solder pastes. Notice the newer paste shows better release characteristics throughout the entire area ratio range that was measured (0.4 to 1.0).

The current pastes also exhibit a curve with a different shape. This curve looks like the upper quadrant of a circle, whereas

the previously generated curve was a polynomial S-shape. Therefore the equation that models the circle has a different algebraic format than its predecessor.

Regression analysis of the data produced an R value of 0.929, showing a high degree of correlation. The regression coefficients that were generated were: slope= -3.008, and y-intercept= 0.995. The data and trendline is shown in figure 9.

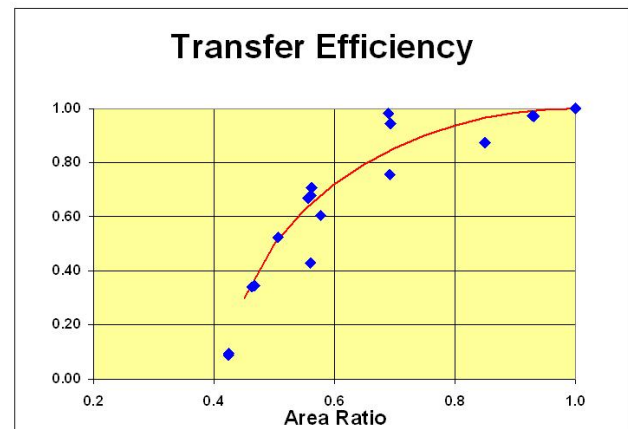


Figure 9. Plot of transfer efficiency vs. area ratio showing scatter about the trendline, with R value of 0.929.

It should be noted that transfer efficiency models are only generated for straight (normal taper) apertures. Data from steps or microsteps are not included in the calculations. No models for stepped or microstepped apertures have been generated.

It should also be noted that registration of the microstep is a critical factor in the manufacturing process. In order to achieve registration of 0.0005" or less, manufacturing is performed under extremely tight tolerances and many in-process measurements are taken.

CONCLUSIONS

The fine feature print performance of the lead-free and tin-lead solder pastes were nearly identical. The widespread notion that assemblers cannot expect lead-free pastes to print as well as tin-lead pastes is a myth. This study tested one of the most difficult to print scenarios – 10 mil features with type 3 pastes.

The data generated in the print tests can provide an easy reference to aid in stencil design and foil thickness selection, based on the need for varying thicknesses driven by PWB layout. Because the data was generated on a PWB in a production-type setting, the reader can anticipate similar results on his or her assembly line.

The transfer efficiency models show definitive improvement in release characteristics in newer paste formulations, when compared with similar tests performed in 2001.

Microsteps can enhance transfer efficiency in specific situations where area ratios are very low. Transfer efficiency models have been generated for standard apertures based on area ratio, but models have not yet been developed for microsteps.

RECOMMENDATIONS FOR FUTURE STUDIES

The advantages of the MicroStep pocket design should be studied in more depth. Particular factors of interest are the depth of the pocket, the separation speed of the stencil, and the formulation of paste used. On the 5 mil foil, the microstep was 2 mils deep, and did not show a discernable advantage. On the 4 mil foil, the pockets were only 1 mil deep, and did show a definite advantage. The effect of step depth should be studied in greater detail.

The engineers who performed the print tests felt that a slower release may also improve the deposit volumes and consistencies. A very fast separation speed was used in this study because it has historically been shown to be most effective with straight wall apertures with the two paste formulations that were used. Very little data is available to optimize separation speeds for stepped or microstepped areas.

It is also theorized that prior-generation solder pastes could benefit more from the use of microstep pockets. The newer formulation pastes that were used in this study (the same ones that perform better with faster snap-off speeds) were designed with fine feature stencil release in mind. Their release characteristics were shown to be superior to earlier formulations. The more mature formulations that need a little more coaxing to release from the stencil may realize greater incremental improvements from the use of MicroSteps than the modern products.

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