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SURFACE MOUNT ASSEMBLY AND BOARD LEVEL RELIABILITY FOR HIGH DENSITY POP (PACKAGE-ON-PACKAGE) UTILIZING THROUGH MOLD VIA INTERCONNECT TECHNOLOGY

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ABSTRACT

This paper addresses the recent technological advancements made in the areas of 3D packaging, surface mount and package stacking for next generation high density Package-on-Package (PoP) applications. The PoP architecture integrates high performance logic devices in the bottom package and high capacity or combination memory devices in the top package through a flexible 3D packaging platform. PoP has become an effective solution for smartphones, digital cameras and personal media players due to the flexible integration and business model benefits package stacking provides. As these handheld products converge, the increased functionality will require higher signal processing performance with increased data storage capability thereby increasing interconnection and signal integrity challenges. Next generation PoP technologies must handle these challenges with continued miniaturization, supporting higher interconnect density in a thinner structure with improved warpage control.

Convergence of functions in handsets is driving requirements for smaller, thinner, higher density PoP stacks that are projected to exceed the capability of current bottom package stackable technologies. The standardization of the memory interface has accelerated PoP adoption, but to support the increased functionality in convergence products, a next generation bottom package technology is required that provides a higher density memory interface that will support low power DDR2 and non volatile memory architectures. The future memory interface must enable higher data transfer rates, wider bus and higher memory capacities - resulting in the need for a finer pitch, higher density interface between the stackable packages. Ideally the next generation bottom package platform will allow the memory interface to scale with fine pitch BGA pitch trends without requiring new SMT processes to be developed. Trends in logic devices are driving integration of multi band modems and application processors that operate at higher clock speeds. This integration can be provided in dual die or dual core solutions. Either solution increases signal processor functionality, pin count and interconnect density - creating packaging and signal integrity challenges by themselves but further complicated for PoP applications due to the future memory interface challenges introduced above. Thus, the next generation bottom PoP technology must support, dual die (including stacked die) for wire bond or flip chip devices in addition to passive component integration for improved signal integrity while providing a flat and scaleable high density memory interface.

This paper summarizes the new mechanically-balanced bottom package structure that Amkor presented at ECTC this past May. This paper describes how this new package addresses the current and next generation PoP requirements by the use of a solderable through mold electrical interconnect structure. This paper provides data from a warpage control, SMT stacking and board level reliability joint study between Amkor and Sony Ericsson Mobile Communications (SEMC). Board level reliability performance improvement is demonstrated by comparing this new package structure with a conventional exposed thin die flip chip bottom stackable package. A 14 x 14mm (less than 1.4mm thick) PoP test vehicle was developed using a six net daisy chain design to fully evaluate the mechanical reliability of first and second level interconnects. The test vehicle provides two nets for the 620 bottom BGAs at 0.4mm pitch, two nets for the 200 pin top interface at 0.5mm pitch and separate nets for the thin daisy chain FC die. In addition, the test vehicle used 01005 sized zero ohm resistors to represent decoupling caps. This paper also summarizes the PoP size reduction that can be achieved for the benefits of a memory interface technology that can scale to 0.3mm pitch requirements.

Key words: 3D packaging, package on package, PoP, package stacking, through mold via, TMV™, warpage control

INTRODUCTION

PoP shipments more than doubled in 2007 to over 140 million units [1] driven by strong adoption in smartphone applications where high semiconductor content puts PWB area at a premium. Continued strong demand for smartphones is being forecasted as an increasing number of business professionals and consumers require the high speed connectivity and multimedia content that these feature-rich handsets provide.

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Future smartphone designs demand higher performance signal processing and high speed memory architectures that will require higher density PoP technologies.

Summary of Next Generation PoP Requirements

The macro trends for PoP match those of handheld systems – smaller, thinner, and lighter, with higher performance at a lower total cost of ownership. But a clear understanding of the system and device drivers is required to select and develop a robust next generation PoP technology platform [2].

System level requirements

- Reduced PoP footprint and stacked height.
- Reduced bottom package warpage for fine pitch SMT stacking using existing processes.
- Capability to integrate decoupling capacitors within the bottom package to manage high speed or noise sensitive signals.
- Higher density stacked memory interface between the two packages.
- Improved solder joint reliability of the PoP stack without component underfill

Processor device requirements

- Dual core processors that integrate baseband modem and application processor blocks, which increase I/O and require higher interconnect densities.
- Higher speed processor that can exceed 1 GHz with more complex memory controllers, which drive tighter signal integrity and timing budgets.
- Transition to 65nm and 45nm low power process nodes to enable higher CMOS integration and performance at lower cost.
- Utilization of flip chip interconnects for improvement in electrical performance, reduced IR-drop, increase in I/O density and reduction in package size.
- Integration of dual-die in one package to enable partitioning of digital and analog functions, add a high speed modem chip to an existing baseband or enable baseband plus application processor die combinations.

Memory device requirements

- Higher speed RAM - from SDRAM to low power DDR to low power DDR2.
- Wider bus width from 16 to 32 bit and from shared to split, to 2 channel bus architectures that require higher pin counts.
- Increased capacity for both RAM and Flash memory, drive larger die or more die in the stack.
- Expanded memory architecture flexibility, so that a single memory interface supports a wider range of memory combinations.

The above system and device drivers can be combined into the following set of key next generation PoP technology requirements.

- High density memory interface that will scale with memory architectures, without requiring new stacking process development.
- Tighter warpage control for high stacking yields with fine pitch components, without PoP thickness reduction limitations.
- A bottom package platform that can support wire bond, flip chip, dual die, stacked die and passive integration requirements without expensive new tooling or process development.

Figure 1 illustrates the current single chip bottom logic package platforms in volume use today and their shortcomings in meeting the above next generation requirements.



Structure 1. Bottom package - wire bond, center gate mold package structure: has warpage control, thickness, die size, dual or stacked die, passive integration and memory interface density limitations.



Structure 2. Bottom package - flip chip, exposed die package structure: has warpage control, underfill bleed, stacked die and handling limitations.

Figure 1. Structure and Limitations of Current Bottom PoP Technologies

Wire bond designs dominate the current class of baseband or application processor devices, thus structure 1 represents the bulk of 2007 PoP stacks. At the 65nm node there has been a strong transition to flip chip designs as shown in structure 2, to meet the I/O density and electrical performance requirements. Both of these bottom PoP structures have cost and technical limitations which would require major trade off concessions to apply current technologies to the range of next generation PoP requirements. Technical evaluations and feasibility studies have been conducted on a host of solutions to meet challenging next generation requirements; including:

- Extremely thin die (≤ 50um) with thin die attach and ultra low loop wire bonds, under very thin 0.2mm mold caps that can support 0.5mm pitch stacking. However,

redesign and retooling is required below 0.5mm pitch and wafer thinning and die handling of such extremely thin die can cause mechanical / electrical performance or assembly yield challenges.

- Build up substrate technologies that provide a partial cavity structure for the die to recess below the memory interface stacking pads. However, high cost, limited substrate availability, design and material set restrictions limit this technology's adoption.
- Adding solder balls to the top lands of the bottom package to allow use of current mold caps for finer pitch or taller stacked interface applications - associated with stacked die in the bottom package [3]. This effectively extends the range of the current technology but does not address all of the next generation requirements.
- Memory interface fan-in like structures which apply technologies used in niche package in package structures, but have cost and stack height restrictions. More concerning is this can limit commodity memory and stack height requirements, as would require a new class of extremely thin fan-in memory footprints which suppliers have to offer in addition to current MCP and top PoP components.
- Embedding the processor device in an organic build up substrate or rebuilt / redistributed wafer level process technology, which each have serious cost, yield, infrastructure, new development, capital investment and cycle time limitations.

Each of the above technologies can address a subset of the next generation requirements but have limitations if applied across the range of requirements and future PoP applications. They also have risks in maintaining low unit, development and capital equipment cost structures. Thus, a new technology is required that leverages mainstream package platform roadmaps following lessons learned from the initial PoP development. Where Amkor applied a disruptive but proven technology (center pin gate molding) on the base technologies from mass market fine pitch BGA (FBGA) and stacked die platforms which allowed the PoP (structure 1) to be released to production, just 15 months after concept definition, as reported in an industry article last year. [4]

At ECTC May, 2008 Amkor reported details of a new structure expected to provide scalability to meet next generation PoP requirements. [5] The disruptive but proven technology applied here is laser ablation (referred to as through mold via technology or TMV™) to enable use of matrix molded processing for the bottom package platform.

Methodology in Development of Next Generation PoP Test Vehicle for Joint Study

SEMC has conducted technology projects for a number of years to evaluate the surface mount assembly and board level reliability performance of emerging packaging technologies. Amkor has participated in these projects for years by designing daisy chain components that demonstrate emerging packaging technologies and meet SEMC's next generation requirements for size, thickness, pin count and pitch. For 2007, a technology project was defined to evaluate the surface mount and board level reliability for a high density next generation PoP technology. Design requirements were defined and discussions were held to review technologies which could address the design requirements. Amkor proposed to develop a test vehicle using the emerging TMV™ technology to study against the exposed flip chip die bottom package structure shown as structure 2 in Figure 1 above. Design reviews were held to finalize the design and agree on the design of experiments plan. Figure 2, provides the key elements of the bottom TMV™ package design selected for the project.

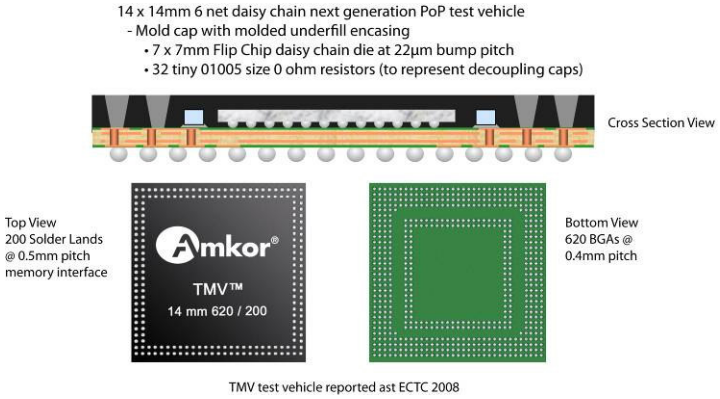


Figure 2. Cross section, top and bottom views of test vehicle for new bottom PoP package technology using TMV™ technology.

The benefits of TMV™ technology for next generation PoP requirements are:

- TMV™ technology removes the pitch vs package clearance bottlenecks to support future memory interface density requirements. Figure 3 shows the PoP size reduction benefits, as TMV™ enables the memory interface to scale with CSP pitch reduction trends.
- TMV™ improves warpage control and bottom package thickness reduction requirements, by utilizing a balanced fully-molded structure.
- TMV™ provides an increased die to package size ratio.
- TMV™ supports wire bond, FC, stacked die and passive integration requirements.
- The TMV™ structure leverages strong technology roadmaps and high volume scale, from FBGA, stacked die, flip chip CSP, and system in a package (SiP) platforms. Integrates proven laser ablation technology available from a host of laser process equipment suppliers.
- The TMV™ structure can improve board level reliability of the stacked memory interface.

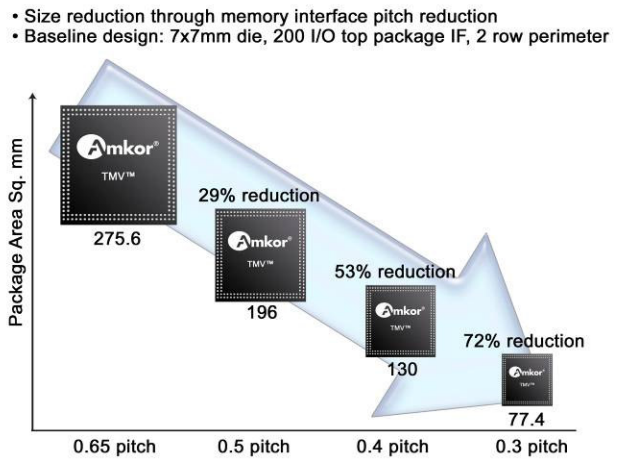


Figure 3. PoP package size reduction through scaleable memory interface enabled by TMV™ technology.

TEST METHODOLOGY

The following warpage measurement and Board Level Reliability (BLR) tests were used to assess the performance of TMV™ PoP.

- Thermal Shadow Moiré warpage testing
- Temperature Cycle fatigue testing
- Cyclic Bend fatigue testing
- Drop Shock testing

Daisy Chain Test Vehicle

A daisy chain test vehicle was designed to simulate a next generation high density PoP stack and to monitor critical electrical paths during BLR testing. Figure 4 and Figure 5 illustrate the 6 networks designed into the test vehicle.

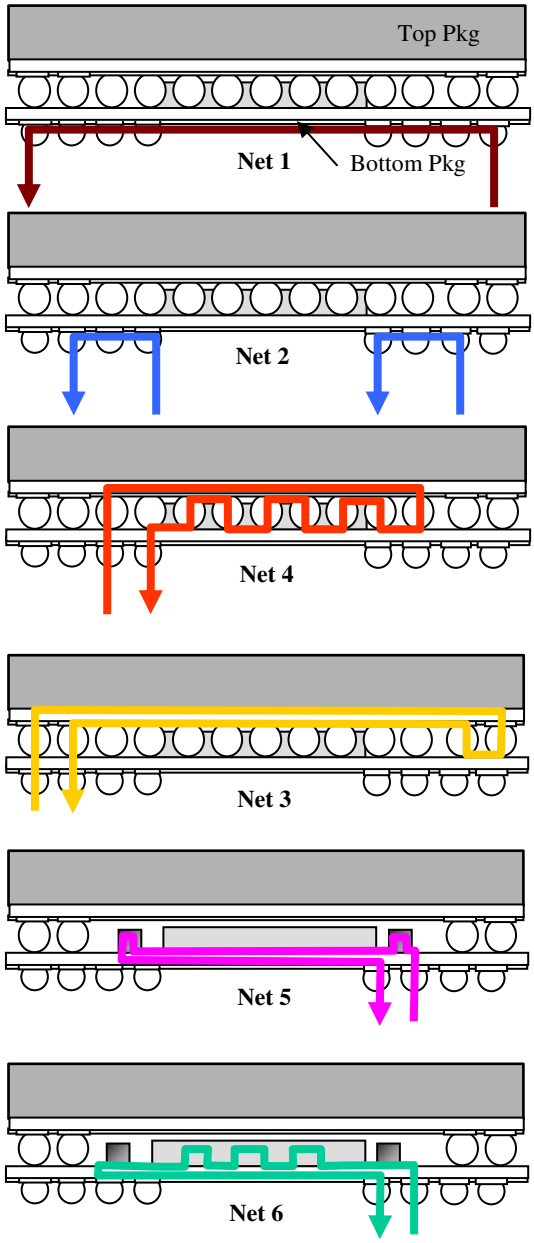


Figure 4. 6-Net PoP Daisy Chain Design

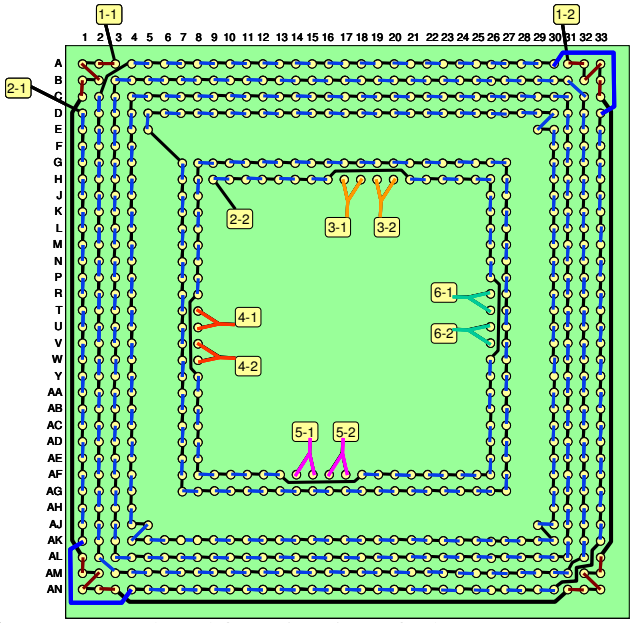


Figure 5. Test board footprint view of 2 bottom BGA Nets and I/O points flagged for upper DC nets. (Black lines are PWB side connections)

Net Descriptions

The networks are described below.

1. Brown line: daisy chain netlist of bottom package, corners ball nets (6 / corner, 24 balls)
2. Blue line: daisy chain netlist of bottom package, primary bottom BGA pattern (596 balls)
3. Red line: daisy chain netlist of top package to bottom package primary memory interface (184 balls)
4. Orange line: 4 / corner net of top memory interface (16 balls)
5. Purple line: daisy chain through 32 passives of bottom package (8 per side around the FC die)
6. Green line: daisy chain through FC silicon DC die of bottom package

Package Construction

The test vehicle for this development is a 14 mm x 14 mm matrix molded bottom stackable package using TMV™ technology, as shown in Figure 6. The bottom footprint is a 33x33 BGA array containing 620 balls at 0.4 mm pitch. The top side contains 200 TMV™ interconnects in a JEDEC compliant 2 row, 0.5 mm pitch perimeter 27x27 array. The base package contains 1 flip-chip daisy chain die. The die size is 7.10 mm x 6.97 mm and die thickness is 0.127mm. The base package substrate is 4 layer 1+2+1 blind and buried via construction with a 0.05 mm thick core and 0.04 mm thick prepreg. Total substrate thickness is 0.21 mm and an existing 0.4mm thick mold cap was used as it was capable of molded underfill process. The resulting overall PoP stacked structure (top + bottom) is 1.36 mm maximum thickness after board mount.



Figure 6. TMV™ PoP Test Vehicle

For comparison, a bare die Package Stackable flip chip CSP (PSfcCSP also referred to as fcPoP) was constructed as a control sample leg in the DOE. In the case of the bare die package, the substrate core thickness had to be increased to 0.100mm thickness for an overall substrate thickness of 0.3 mm due to warpage control requirements based on shadow moiré studies. The bare flip-chip die is underfilled using a capillary flow underfill material whereas the TMV™ technology enabled the mold compound to act as the FC underfill material. For the package stackable exposed FC based structure, the total PoP stack thickness is 1.25 mm maximum after board mount. All other package attributes are identical between the exposed die to the over molded PoP base package.

The top package is a 14 mm FBGA, representative of a standard PoP memory package with 200 balls arranged in a 2 row, 0.5 mm pitch perimeter array with 0.33 mm diameter lead free solder balls (Sn/1.0Ag/0.5Cu). The top package has a 0.13 mm thick 2 layer substrate with 0.06 mm core. The mold cap thickness is 0.40 mm. Surface finish on the BGA pads is electrolytic Ni/Au. The top package contains 8.3 mm x 8.3 mm x 0.152 mm thick dummy die to represent the Si ratio and package warpage of typical combo memory die stacks. [5].

The exposed die PSfcCSP (fcPoP) package stack-up is shown in Figure 7 and Table 1.

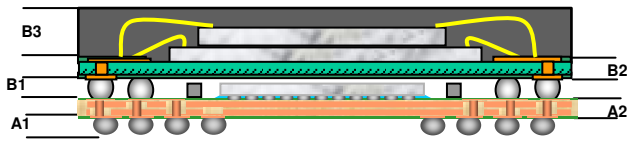


Figure 7. PSfcCSP Test Vehicle

Symbol	unit	SCSP on PSvfBGA		
		Min	Max	Nom
A1 (Mounted, 0.4 pitch)	mm	0.120	0.180	0.150
A2 (4L laminate)	mm	0.270	0.330	0.300
B1 (Stacked, 0.5 pitch)	mm	0.210	0.270	0.240
B2 (2L laminate)	mm	0.100	0.160	0.130
B3 (Mold cap)	mm	0.370	0.430	0.400
Overall Pkg height	mm	1.153	1.287	1.220

Table 1. PSfcCSP Package Stack-up

Printed Circuit Board Assembly

The TMV™ PoP and PSfcCSP test vehicles were assembled to CuOSP-coated printed circuit boards. Both solder masked defined (SMD) and non solder masked defined (NSMD) PCBs were used. Figure 8 illustrates the PCB assembly sequence. A no clean, printed lead free solder paste was used to mount the bottom package to the PCB. A tacky flux was dip applied to the top package's solder balls prior to mounting it to the bottom package. Underfill was not used during the SMT assembly, however, underfill processing was conducted on selected samples but underfill BLR results are not reported in this paper.

PCB Assembly Flow:

1. Screen print solder paste to the PCB
2. Attach bottom package to the PCB
3. Dip top package in flux
4. Mount top package to bottom package
5. Reflow in air environment
   a. Time above liquidus: 60 sec
   b. Peak temp: 243 to 251°C

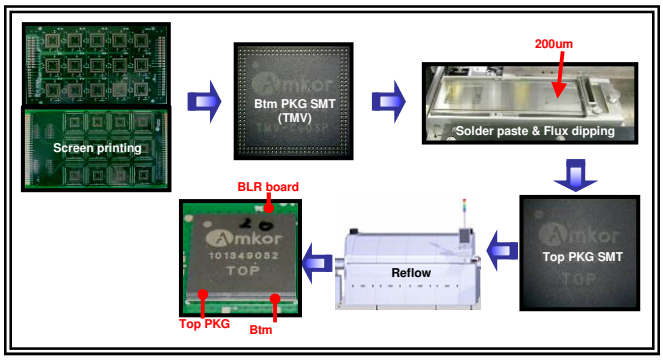


Figure 8. Circuit Brd PoP Stack Assembly Process Flow

An assembled BLR test board is shown in Figure 9.

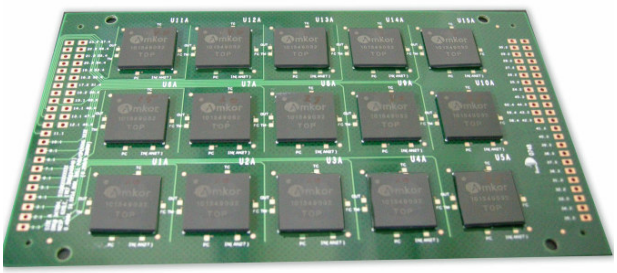


Figure 9. Assembled BLR test board

Figure 10 shows a cross section view of a TMV™ PoP test vehicle mounted to a BLR test board.

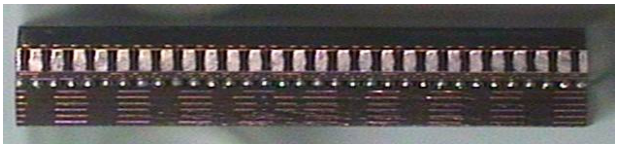
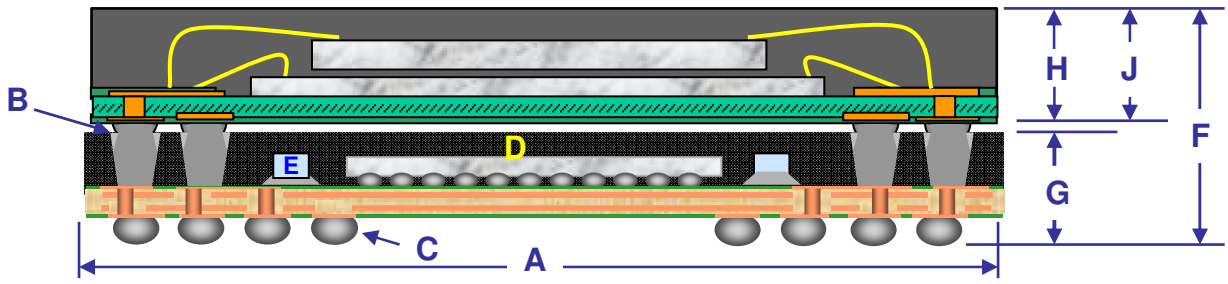


Figure 10. Cross section view of a TMV™ leg PoP stack on the BLR test board

TEST RESULTS

Figure 11 illustrates the construction and package stack-up for the TMV™ PoP Test Vehicle.

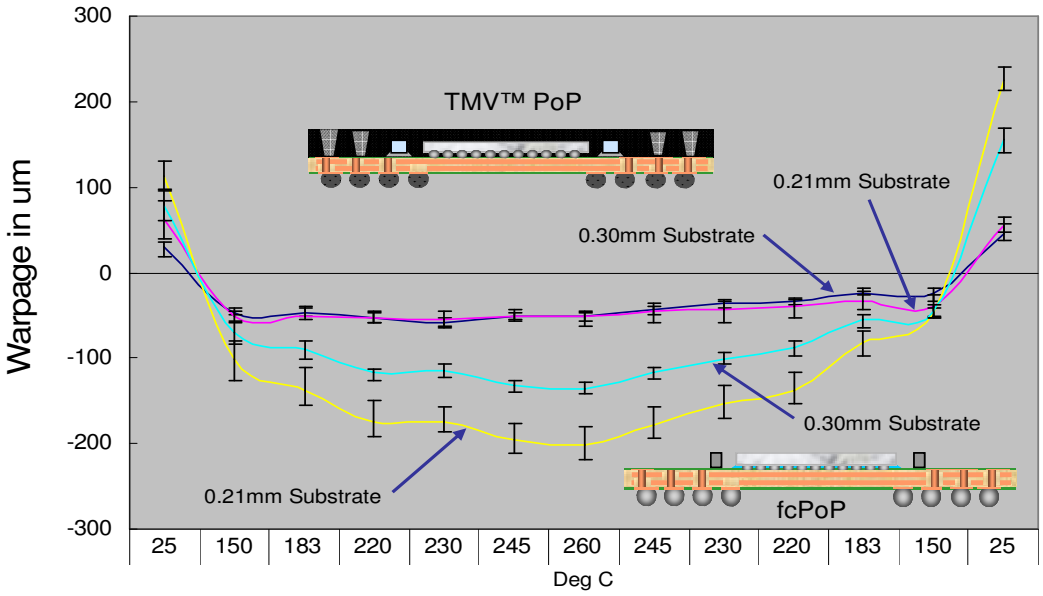


Testing	Body (A)	Foot print – top (B)	Foot print – bottom (C)	Die Size (D)	Passives (E)	Package Stack-up (F) mm
Board Level Reliability (BLR)	14x14mm	0.50mm pitch 200 pad 27 matrix 2 row	0.4mm pitch 620 BGA 33 matrix 4+2 row,	7.100 x 6.970 x 0.13mm	Size: 0105 Qty: 32	Mold cap: 0.40 Substrate: 0.21 Ball Ht: 0.15 Btm Pkg Ht (G): 0.76 Gap (H): 0.03 Top Pkg Ht (J): 0.53 Tot Pkg Ht (F) 1.32

Figure 11. Board Level Reliability Test Vehicle Description

Warpage Performance

Thermal Shadow Moiré testing was performed to evaluate the warpage of the test vehicles. The TMV™ PoP package exhibited a dramatic improvement in warpage compared to the conventional PSfcCSP package, as illustrated in Figure 12. A thicker 0.3mm substrate was required to improve the warpage in the PSfcCSP configuration. PSfcCSP samples with the extremely thin core 0.21mm thick substrates were judged to have too severe of a warpage profile to be considered for SMT stacking. In comparison, substrate thickness has little affect on the TMV™ PoP test vehicle's warpage. Excess warpage can cause surface mount yield failures during the PoP stacking and motherboard assembly. Thus, warpage is a critical attribute for reliable PoP printed circuit board assembly.



Package / Substrate	TMV / 0.21	TMV / 0.30	fcPoP / 0.21	fcPoP / 0.30
Max warpage (um)	-54.8	-51.8	-202.2	-136.8

Figure 12. Thermal Shadow Moiré Warpage Measurement Plots

Board Level Reliability (BLR) Test Results

There was a very complex design of experiments (DOE) for this project with many variants studied, including:

- 2 different top package warpage profiles
- 2 different bottom package structures
- SMD vs NSMD test board pads
- PoP stack BGA underfill vs no underfill
- 3 different underfill material types

Since the project was forward looking for next generation technology direction and due to the high number of legs and samples tested; failure analysis results were not available to define the location of BLR failures or the failure mode. Very promising BLR results were reported for the TMV™ PoP structure which this paper will summarize in the following figures and explanations.

Thermal cycle test results are shown in Figure 13 for NSMD test boards without underfill. The cycle at first failure and the characteristic life have been plotted for each package. (The arrows indicate characteristic life not determined as exceeds 800 cycles). Here the TMV™ PoP had superior performance for both the bottom and top solder joints in both number of cycles to first failure and in the characteristic life. From modeling results and experience we attribute improved top joint life to the mechanical benefits associated with the TMV™ stacked interface which reduces stress at the critical bottom

interface of solder joints between the packages. As was reported in a previous high density PoP study [3], fine pitch stacked interfaces can show a high number of early drop failures at the lower interface of the stacked solder joint due to the higher bending stress than the upper interface experiences. In addition we theorize the TMV™ structure can increase bottom solder joint life due to two factors. First overmolding of the FC die can reduce the stress concentration on BGAs under the die edges. In bare FC die package structures, solder balls under the die and near the die edges see the highest stresses and fail first. The molded underfilled structure of TMV™ can reduce the stress concentration to improve temp cycle life. The second theory is due to the warpage control benefits the TMV™ structure provides. Warpage control enables more consistent and robust solder joint formation in the SMT process which can reduce stress concentration on the thinner / stretched solder joints typical at the corner of BGA packages that have high concave (package smile shape) warpage profiles at the liquidus temperature as reported in Figure 12.

Note, Amkor is conducting additional BLR tests on this TMV™ PoP test vehicle including failure analysis which we plan to report in a 2009 paper.

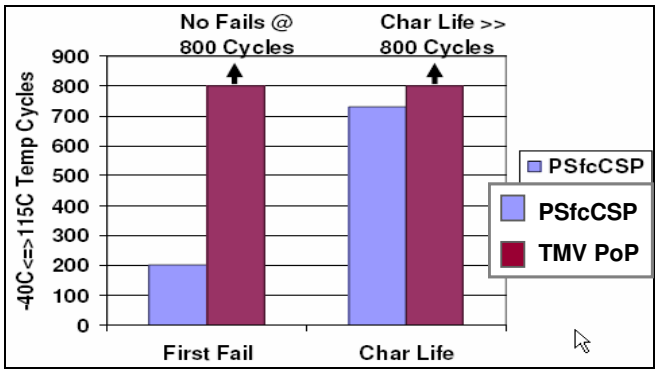


Figure 13. Thermal Cycle Test Results, NSMD Pads

Thermal Cycle Test Summary

- -40°C to 115°C, 2 cycles/hr
- Bottom BGAs typically failed first
- TMV™ PoP showed superior thermal cycle BLR performance

Cyclic Bend Test Results

The Cyclic Bend test results are shown in Figures 14 and Figure 15 for NSMD and SMD PCB's again without underfill. In both cases, as with thermal cycle testing, TMV™ PoP showed superior performance. Again without fail location and mode FA results we looked to modeling and experience to explain the results. First we attribute improved top joint results to the TMV™ package's fully-molded construction that mechanically supports the top solder joints and increases bottom package stiffness to reduce the bending stresses between the top and bottom packages. Secondarily the improved warpage control the TMV™ structure provides, allowed use of a thinner bottom substrate which has lower stiffness, which models indicate reduce stresses on bottom solder joints.

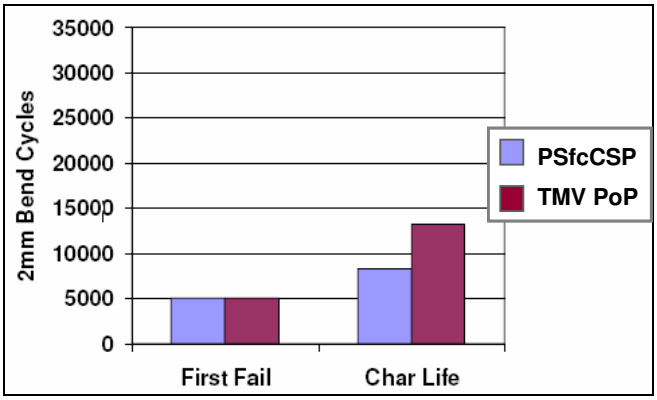


Figure 14. Cyclic Bend Test Results, NSMD Pads

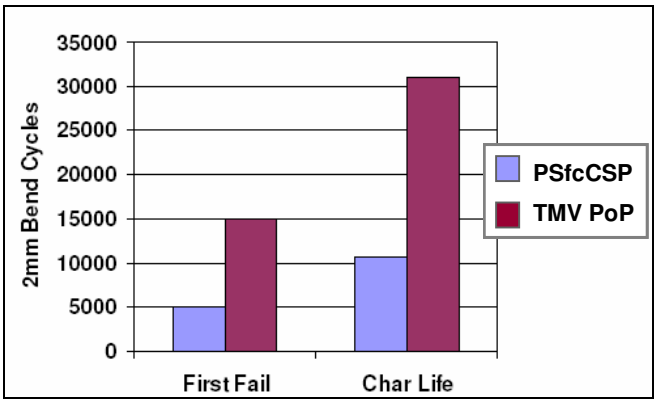


Figure 15. Cyclic Bend Test Results, SMD Pads

Cyclic Bend Test Summary

- JESD22-B113, 2mm Displacement
- Bottom BGAs typically failed first
- TMV™ PoP showed superior cyclic bend performance

Drop Test Results

The Drop Test results are shown in Figure 16 for SMD boards without underfill. Both packages exhibited impressive performance with all units under test passing in excess of 40 drop cycles. However, due to the high number of legs studied drop testing was not carried out beyond 40 drops in order to determine if there are performance trends by package type. (This work is underway on a follow up study). To understand the mechanical benefits of the TMV™ structure, mechanical drop life simulations were run to JEDEC standard drop test loading conditions. Sub-modeling was conducted to transfer boundary conditions from board level dynamic response to the local 3D component model to give detailed analysis of critical solder joints. Accumulated plastic strain at critical solder joints was used as damage

indicators to correlate to drop performance. Figure 17 shows greater than a 2x improvement on mean drop life as simulated for the top solder joints in the TMV™ structure vs the mean life for the bottom solder joints.

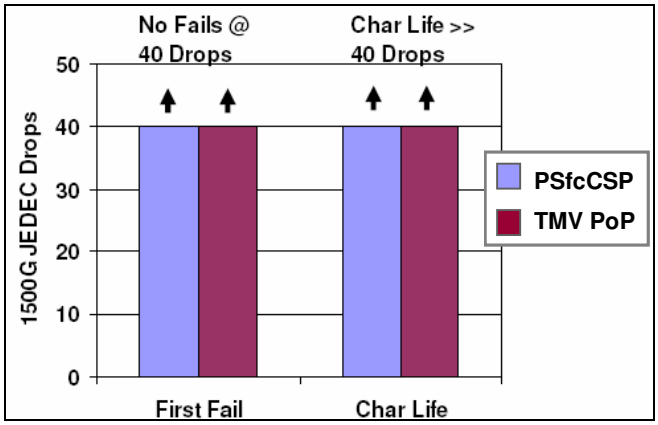


Figure 16. Drop Test Results, SMD Pads

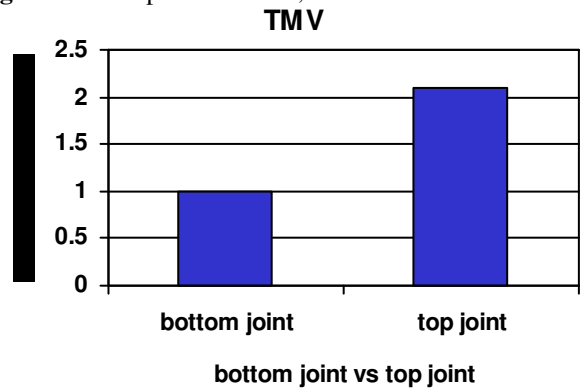


Figure 17. Drop life simulation for TMV™ Structure

As can be seen in Figure 18, the TMV™ structure provides mechanical support to the critical bottom interface of the stacked solder joint shown in red through the mold compound of the bottom package shown in gray. Drop modeling predicts 20 – 30% life improvement in top solder joint for TMV™ structure when compared to the unsupported structure associated with convention PoP stacked technologies. The molded structure of TMV™ helps in reducing the relative bending between the top and bottom packages, thus reducing the stresses in top joints. The drop reliability can further be optimized by combining the structure benefits of TMV with an optimum sizing of pad openings for the top package, as the top package solder mask opening does not have to be reduced to provide solder joint stand off clearance over center mold or exposed FC structures in the bottom package.

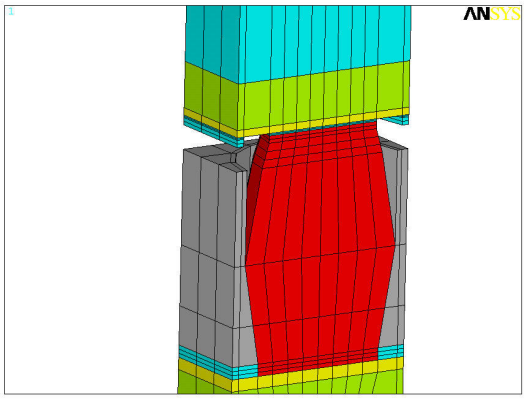


Figure 18. FE Model of top solder joint with TMV™

CONCLUSION

A new bottom package technology and structure was developed that addresses the density challenges associated with next generation PoP applications. A 6 net test vehicle was developed for joint study to compare the new structure that utilizes through mold via interconnect technology against a current PoP technology where the flip chip die is exposed to reduce die height above the stacking pad interface. Fine pitch PoP stacking was achieved by SEMC utilizing current flux dip on pass reflow SMT stacking processing. The new bottom package structure with TMV™ technology showed superior package warpage control capability allowing the use of extremely thin core substrate technologies. The new bottom package structure with TMV™ technology demonstrated improved board level reliability results.
Amkor has extensive ongoing BLR testing for this test vehicle to be reported in a future technical paper.

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TMV is a trade mark of Amkor Technology, Inc.

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REFERENCES

[1] Advanced Packaging Update: Market and Technology Trends, Volume 4, March 2008; TechSearch International.

[2] Lee Smith, "Driven by 'Smartphones,' Package-on-Package Adoption and Technology Are Ready to Soar," Chip Scale Review, July 2008.

[3] Moody Dreiza, Akito Yoshida, Kazuo Ishibashi, "High Density PoP (Package-on-Package) and Package Stacking Development," Proceedings of The 57th Electronic Components and Technology Conference, Reno, Nevada, May 2007.

[4] Lee Smith, "Package on Package: The Story Behind This Industry Hit," Semiconductor International, June 2007.

[5] Jinseong Kim, et al, "Application of Through Mold Via (TMV) as PoP Base Package," Proceedings from The 58Th Electronic Components and Technology Conference, Lake Buena Vista, Florida, May 2008.