Impact of Heatsink Attach Loading on FCBGA Package Thermal Performance

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ABSTRACT

Flip-Chip Ball Grid Array (FCBGA) packages are prevalent in wide range of electronics applications including gaming consoles, mobile gadgets, telecommunications etc. The microelectronics industry is actively shifting towards smaller node sizes (32 nm, 28 nm etc.) and integrating multiple functionalities onto the die. This in turn increases the die power levels and more importantly drastically increases the die heat-flux densities. External heatsinks are typically needed in order to support high thermal power dissipation.

The focus of this paper is to understand and quantify the impact of heatsink tilt on board-level thermal performance. This in turn impacts the overall thermal performance as higher TIM-II bond line thickness results in greater thermal resistance. For high power applications (>50W) wherein the desired system thermal resistances are very low (θ_{ja} < 1 C/W), controlling the TIM-II thermal resistance is critical to achieve an overall low system thermal resistance.

Experimental measurements were performed using a high power FCBGA thermal test vehicle (TTV). The scope of this study includes performing thermal measurements to understand the impact of the following on board-level thermal performance:

1. Package type: Bare Die FCBGA, Molded FCBGA & Lidded FCBGA
2. Impact of uneven heat-sink loading

A novel method for characterizing TIM-II thickness variation is presented in this work. Upon characterizing the TIM-II BLT thickness variation, experimental measurements were performed to quantify the impact on the board-level thermal performance. Finally, merit analysis of the various package types in achieving low overall package thermal resistance will be presented.

KEY WORDS: thermal interface materials, FCBGA, warpage, molded FCBGA, lidded FCBGA

NOMENCLATURE

L_{pin}	pin length, m
h	heat-sink base thickness, m
L_{die}	die length, m

Greek symbols

δ	TIM-II local thickness (m)
ΔZ	Pin height above heatsink base (m)
θ	Thermal resistance (C/W)
α	Constant

Subscripts

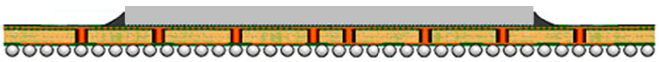
pin	pin
b	heat-sink base
die	die

Introduction

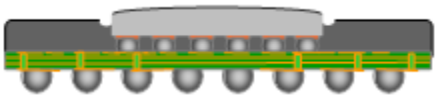
Thermal interface materials (TIMs) are widely prevalent in the electronics industry for reducing the thermal resistance from the source to the external ambient. The TIM thermal resistance is dependent on the bond line thickness (BLT). The inherent warpage of the mating surfaces usually results in a non-uniform BLT in the region of interest for thermal dissipation which is typically directly above the die for FCBGA packages. In a previous study by Dean & Gettings [1], it has been observed that surfaces with large concavity result in higher TIM thermal resistance. Chiu et al. [2] have studied the impact of controlled warpage on the TIM thermal resistance by creating mating surfaces with pre-defined profiles. Solbrekken et al. [3] developed a thermal tester for testing materials at controlled BLTs and pressures.

For high-power applications, external heatsinks are typically attached to the flip-chip package using various mechanisms such as: i) a thermal gap pad ii) spring loaded retention hardware system with backing plate iii) heatsink brackets etc. The contact surfaces of the external heatsink and the package are inherently warped from the manufacturing process. This in turn results in non-flat surfaces across which the TIM is applied.

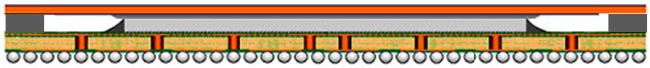
In this study, thermal grease is applied between the package and the external heatsink. Furthermore, a spring loaded system is used to secure the external heatsink onto the package. The focus of this paper is to perform in-situ measurements of the TIM-II BLT directly above the die between the package and the external heatsink. A novel method to perform precision measurements of TIM thickness variation above the die is presented in this paper. Three different flip-chip packages namely: Bare-die FCBGA, Molded FCBGA and Lidded FCBGA were experimentally evaluated using this procedure. Figure 1 shows the three different package configurations.



(a) Bare-die FCBGA



(b) Molded FCBGA



(c) Lidded FCBGA

Fig 1: FCBGA package configurations of interest

In-situ TIM-II Thickness Measurement Procedure

As mentioned in the previous section, spring loaded hardware retention systems were used to secure the heatsink to the package. Figure 2 shows images of the heatsink mounted onto the package and secured to the motherboard using a backing plate. Four springs on the four corners provide the required load for the heatsink mount.

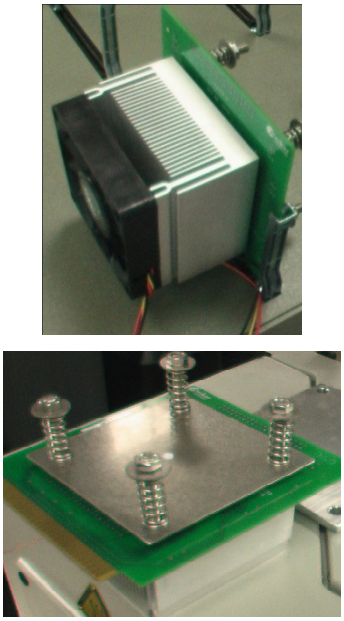
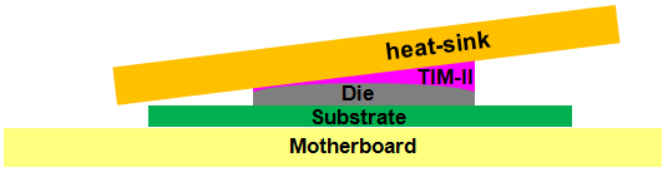
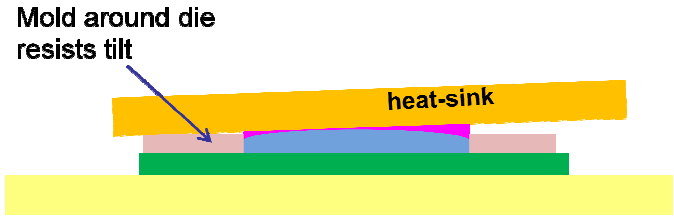


Fig 2: Heatsink mounted to package using spring-loaded retention hardware

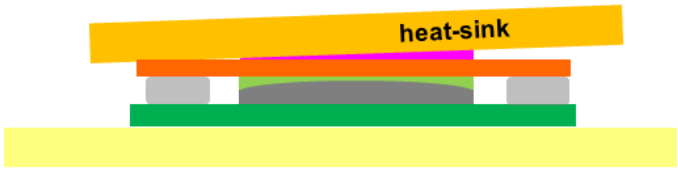
In typical high volume OEM assembly lines, heatsinks are assembled onto the package by compressing the springs (using a nut-driver) to create a required load. Factors such as non-uniform spring constants and varying spring compression lengths on the four corners will result in heatsink tilt over the package surface. This, in addition to inherent package and heatsink warpage results in a non-uniform TIM-II thickness. A schematic of the tilt above the package is depicted for the three different package types of interest in Figure 3. Please note that the tilt is exaggerated in Figure 3 to clarify the point in discussion. It is important to note that the die is exposed in the molded FCBGA package and is typically about 50-60 µm above the mold surface. Intuitively, as seen from Figure 3, the molded and the lidded FCBGA packages would be tilt-resistant in comparison to the bare die package.



(a) Bare-die FCBGA package tilt



(b) Molded FCBGA



(c) Lidded FCBGA

Fig 3: Heat-sink tilt above the package top surface

The TIM-II thickness variation above the surface of the die is critical to dissipating heat from the top of the package. Also, the TIM-II material should be thermally conductive. Thermal greases and gap pads are typically used as TIM-II materials in the industry. Ideally, we would prefer the TIM-II thickness to be as minimal and as uniform as possible. However, that is not achievable in practical application. Therefore, it is important to be able to estimate the local TIM-II variation above the die surface to accurately predict the package thermal performance. For scenarios similar to shown in Figure 2, the overall package thermal performance is determined by three thermal resistances namely: package thermal resistance ($\theta_{package}$) + TIM-II thermal resistance ($\theta_{TIM\text{-}II}$) + heatsink thermal resistance (θ_{hs}). Among these, TIM-II plays a critical role in effectively dissipating heat from the package to the ambient. The TIM-II thermal resistance is given by:

$$\theta_{TIM\text{-}II} = \overline{\boldsymbol{\delta}}/(k_{TIM} * area) \quad (1)$$

where, $\overline{\boldsymbol{\delta}}$ is the mean TIM-II bond line thickness, k_{TIM} is the TIM-II material thermal conductivity and area is the die area for bare-die and molded packages. For lidded packages, the TIM-II area of relevance will be bigger than the die size and could be estimated by the taking the thermal spreading angle from the die to the lid into consideration.

In general, it is very difficult to obtain in-situ TIM-II thickness variation without performing a destructive cross-sectional analysis of the package. A novel procedure to measure the in-situ TIM-II thickness variation is presented

below. The actual procedure to predict the in-situ TIM-II thickness above the die is depicted in Figure 4 below.

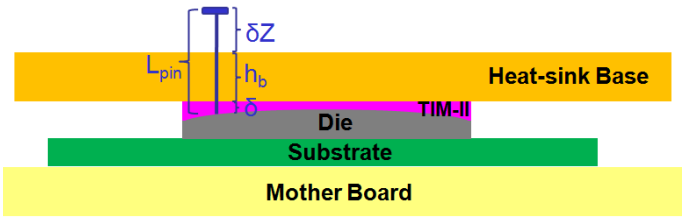


Figure 4: In-situ TIM-II thickness prediction procedure

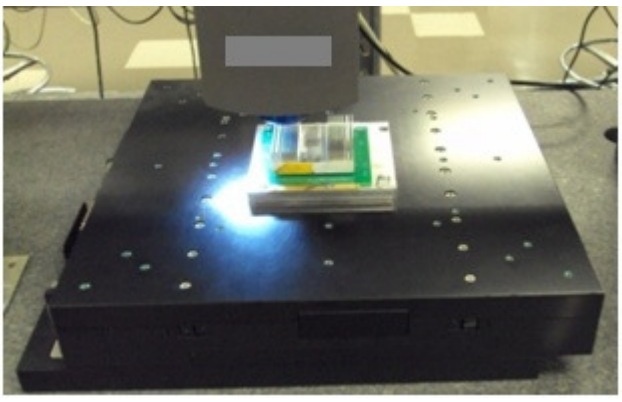
The local pin height $L_{pin}(x,y)$ is measured using non-contact laser profilometer with an accuracy of +/- 1 µm. The pins are slip-fit into a precision ground block (not the heatsink) and the pin height above the top surface of the precision ground block is measured using the laser profilometer. The pin height variation above the surface of the precision block is added to the precision block thickness to estimate the local pin-height.

The pins are then slip-fit into the external heatsink with the pin holes and placed on the profilometer stage. The height variation of the pins above the surface of the external heatsink is measured using the profilometer. This is subtracted from the local pin height $L_{pin}(x,y)$, to estimate the local heatsink base thickness $h_b(x,y)$.

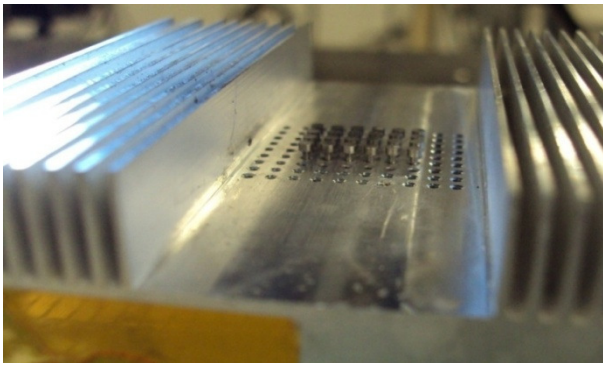
Finally, the heatsink with the precision pins is mounted atop the package and the pin height variation above the heatsink base $\Delta Z(x,y)$ is measured using the laser profilometer. The local TIM-II thickness $\delta(x,y)$ is then estimated using the below equation:

$$\delta(x, y) = L_{pin}(x, y) - h_b(x, y) - \Delta Z(x, y) \qquad (2)$$

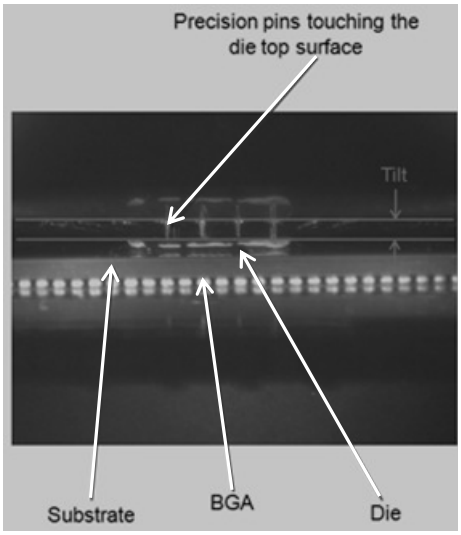
In order to accurately measure the in-situ local TIM-II thickness, precision pins were machined at Core Pins Inc. Pin holes were created in the external heatsink to slip-fit the precision pins. Figure 5 shows images of the precision pins slip-fit into the heatsink and touching the top surface of the die in the side-view image.



(a) Non-contact laser profilometer scanning the pin top surface and the heatsink base



(b) Precision-pins slip-fit in the heatsink



(c) Side-view image depicting the precision pins touching the die top surface

Figure 5: Package tilt prediction procedure set-up

To check the accuracy of the above procedure, the warpage of bare die FCBGA and a lidded FCBGA package was evaluated. Firstly, the package top surface warpage was measured by directly scanning the top surface using the laser profilometer. Later, the package warpage was estimated using the procedure described above. The measurements were repeated three times on each package type. The summary of the measurements is shown below in Table 1.

Table 1: Warpage measurements summary

		Warpage (µm)	
Package	Repetition	Laser Profilometer Direct Scan	Precision Pins
Bare die	1	16	21
	2	16	19
	3	17	20
FCLBGA	1	17	18
	2	17	19
	3	19	18

As seen from the above the table, the precision pin procedure was able to predict the package warpage within reasonable accuracy of the laser profilometer. The standard deviation of the measurements was ~ 1µm.

Experimental Testing

A thermal test vehicle (TTV) was developed to compare the thermal performance of the three different package types: Bare die FCBGA, Molded FCBGA and flip chip lidded ball grid array (FCLBGA) package. The bare die packages were assembled at Amkor factory assembly line. The molded packages were prepared at Amkor thermal test lab using a mold prototype. This resulted in molded surface being about 200-300 µm lower than the die top surface. In contrast, factory assembled packages using production mold chases would result in fairly flat mold surface of about ~50 µm below the die surface. The lidded packages were created by snapping a 0.5 mm Cu lid onto the package using a TIM-1 material.

A description of the package is provided in Table 2. Thermal die equipped with heating elements and diodes as shown in Figure 6, were used to power the die and sense junction temperatures.

Table 2: TTV design details

Body (mm)	31 x 31
Die Size (mm)	10.16 x 12.7 x 0.52
Substrate	3-2-3, 1 mm thick
Cu Lid Thickness (mm)	0.50

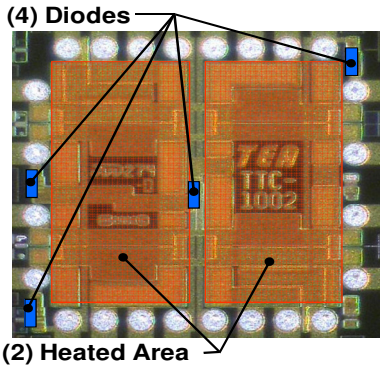
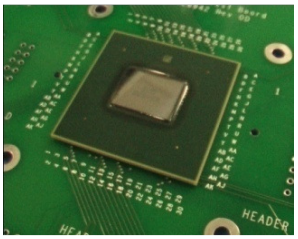


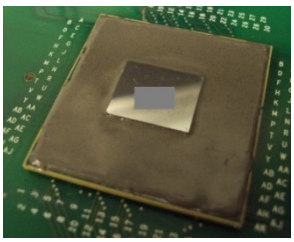
Figure 6: Thermal test die unit cell (2.54mm x 2.54mm)

A 4x5 array of unit cells were used to fabricate the 10.16mm x 12.7mm die. Power to each cell may be controlled independently to study the impact of hot spot size and location on the peak junction temperature. A total of 80 thermal sensors are available to map out the temperature distribution. However, only 37 diodes were used for making temperature measurements on the die.

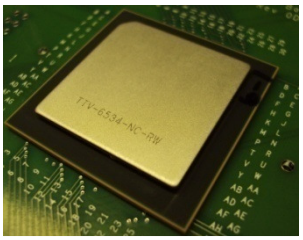
Bare die FCBGA, molded FCBGA and FCLBGA package TTVs mounted to thermal test boards are shown in Figure 7. The exposed die on the molded FCBGA is above the mold compound top surface ensuring that the external heat sink makes contact with the die first producing a thin BLT.



(a) Bare-die FCBGA TTV mounted to test board



(b) Molded FCBGA TTV mounted to test board



(c) FCLBGA TTV mounted to test board

Figure 7: Various package styles tested in this study

TIMs are applied using a screen printing process to accurately control the thickness and area of material. TIMs are dispensed on one side of the stencil and then spread to a 16mm x 16mm area at a thickness of 4 mils using a squeegee. A well defined TIM application is shown in Figure 8.

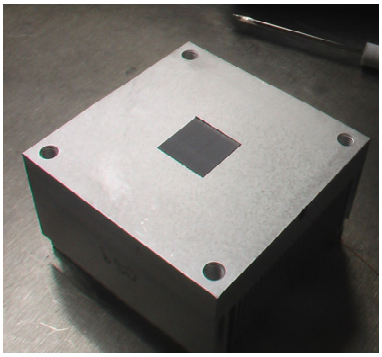


Figure 8: TIM applied on heatsink base

A spring actuation method was devised to avoid board tilting and to ensure a repeatable clamping pressure. First, TIM is screen printed to the heat sink. Second, threaded rods are screwed into the heat sink base. Third, the mother board is aligned using the 4 bolts pressing the die into the TIM. Fourth, springs are inserted along with washers and nuts. Fifth an alignment plate is positioned over the 4 bolts, nuts and washer assembly. Sixth, a mechanical load machined

is used to compress the springs to the desired load (~66N for measurements in this work). The alignment plate is removed and the heat sink is now clamped to the motherboard with the desired clamping force as shown in Figure 2.

Power supply systems were developed to power cycle individual packages. Assembled boards with heat sinks were connected to the power supply system using 60 pin edge connectors. The mother board was tested in a vertical orientation. The packages were supplied with a constant power of ~50W. The steady state thermal resistances were determined with constant power after confirming that all the diode temperatures reached a point of equilibrium. Equilibrium was confirmed at the point where neither the die nor heat sink temperature deviated by more than ±0.2C about the mean value for a 5 minute period. Once equilibrium was reached, temperatures were measured at all 37 die locations, heat sink case temperature, supply current and voltage (measured at die) to each TTV. Power was calculated as the product of current and voltage.

Results and Discussion

The thermal test DOE is shown below in Table 3. The heatsinks will be assembled onto the packages with: i) uniform loading – all springs compressed equally to achieve uniform load of ~16.5 N per spring and ii) non-uniform loading by compressing one of the springs different from the other three springs. All springs were first compressed to achieve uniform load of ~16.5 N. One spring (at a fixed corner for all parts) was then relaxed to achieve half the compression load of ~8.25 N. In-situ measurements were performed to estimate the TIM-II thickness variation above die and typical results are shown in Figures 8, 9 and 10 for the three package styles.

Table 3: Thermal Test DOE

Leg	Package Type	# Packages	Tilt Condition	Test Condition
1	Bare Die	4	Uniform Loading	T = 0, Post Power Cycling
2	Bare Die	4	Nonuniform Loading	
3	FC^{M}BGA	4	Uniform Loading	
4	FC^{M}BGA	4	Nonuniform Loading	
5	FCLBGA	4	Uniform Loading	
6	FCLBGA	4	Nonuniform Loading	

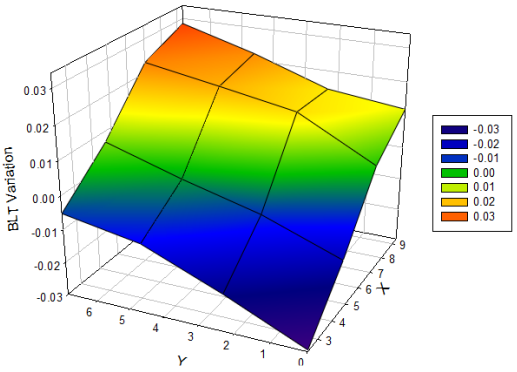


Fig 8: Bare die package TIM-II thickness variation above die

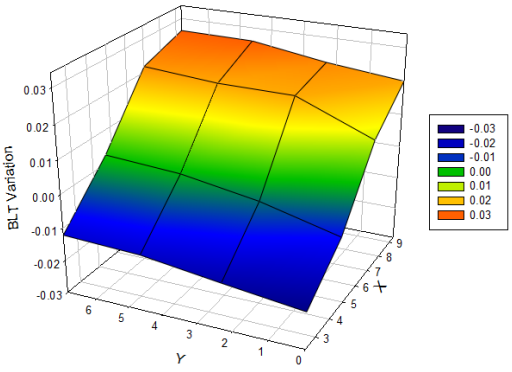


Fig 9: Molded FCBGA package TIM-II thickness variation

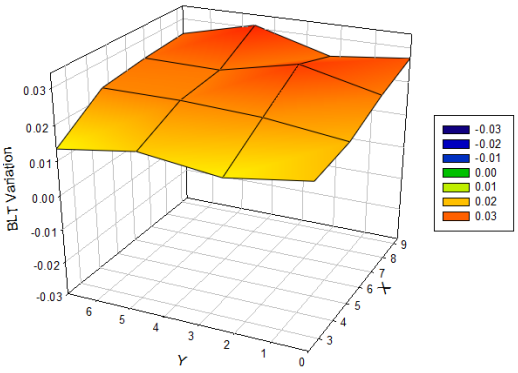


Fig 10: Lidded FCBGA package TIM-II thickness variation

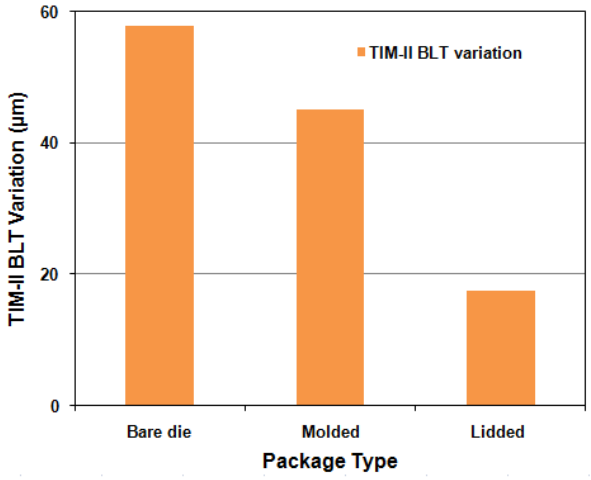


Figure 11: Comparison of max. TIM-II thickness variation

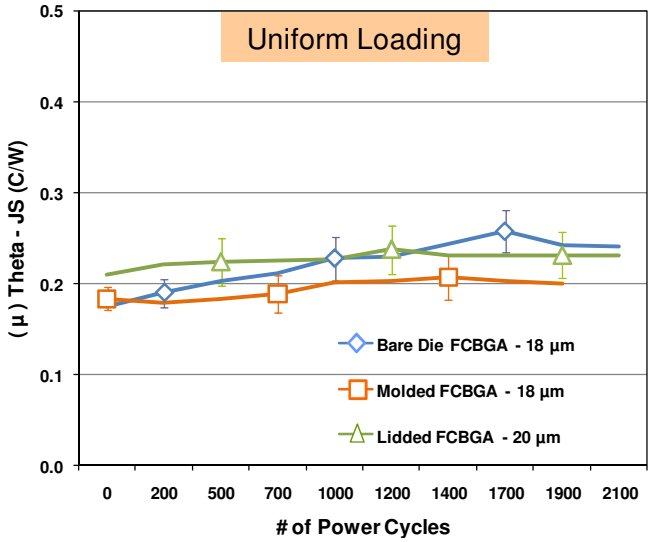


Fig 12: Package thermal performance comparison under uniform loading

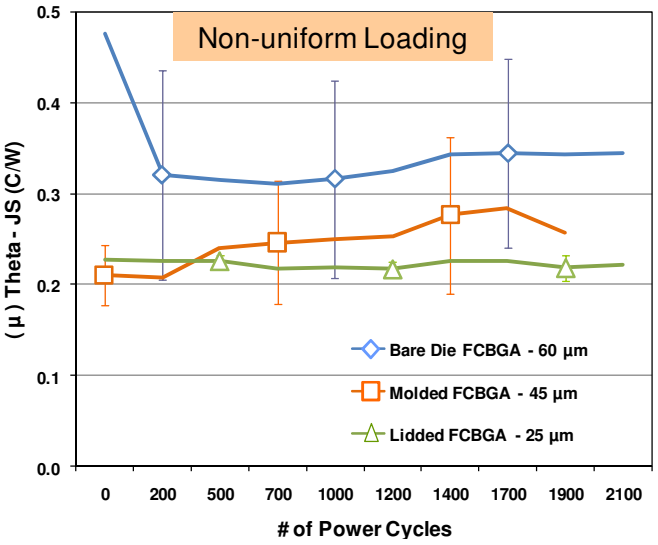


Fig 13: Package thermal performance comparison under non-uniform loading

The maximum TIM-II bond line thickness variation data summarized in Figure 11 show that the molded package resists heatsink tilt in comparison to the bare-die package. θ_{js} (junction to heatsink base) measurements were recorded for all the packages. The junction temperature was estimated based on the maximum temperature recorded among the 37 diode sensors. As seen from the results, the packages with non-uniform loading showed higher thermal resistance in comparison to the packages with uniform loading. The mean θ_{js} measurements among the three different package types with uniform loading are compared in Figure 12. As seen in Figure 12, all packages have comparable thermal performance under uniform loading condition. However, under non-uniform loading condition, the molded package thermal performance is better than the bare die package as shown in Figure 13. There was an initial settling period for the non-uniform loaded bare die parts at T=0 which showed high θ_{js}. The temperature difference (die temperature minus heatsink base temperature) contour plots showing the variation of the temperature across the die is depicted in Figures 14, 15 & 16 for all the package types.

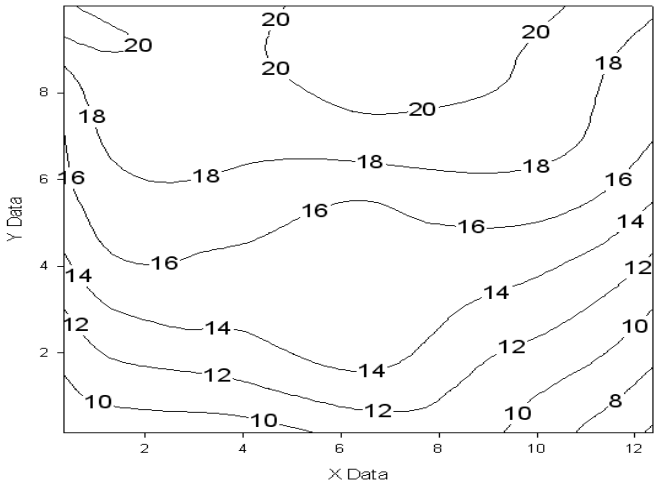


Figure 14: Bare die package ΔT (diode temperature – heatsink case temperature) variation under non-uniform loading

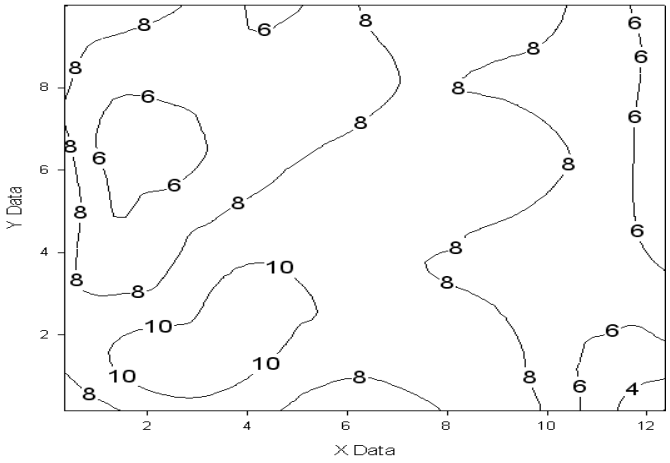


Figure 15: Molded package ΔT (diode temperature – heatsink case temperature) variation under non-uniform loading

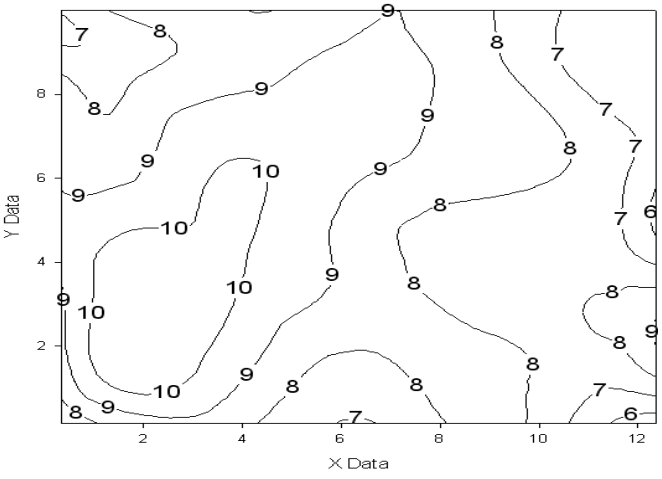


Figure 16: Lidded package ΔT (diode temperature – heatsink case temperature) variation under non-uniform loading

As seen from the above contour plots, it is clear that the variation in the die temperature is highest cross the bare die package. The higher temperatures also agree with the heatsink tilt orientation – in particular for the bare die package.

A 2-D analysis of the package tilt under non-uniform loading is performed below. The die warped profile is assumed to be parabolic as shown below in Figure 17. As mentioned before, the mold around the die resists the heatsink tilt under non-uniform loading. Under extreme non-uniform loading, the heatsink would bottom on the mold top edge which is at an elevated level in comparison to the substrate top edge. This is depicted using the solid magenta line in Figure 17 below. On the other hand, in the case of the bare die package, the heatsink is free to tilt/rotate until it touches the substrate top edge. This is depicted using the green dotted line in the Figure 17. The important thing to note below is that in the case of bare-die package the heatsink bottoms/contacts the die a location further away from the die-center line as compared to the molded package.

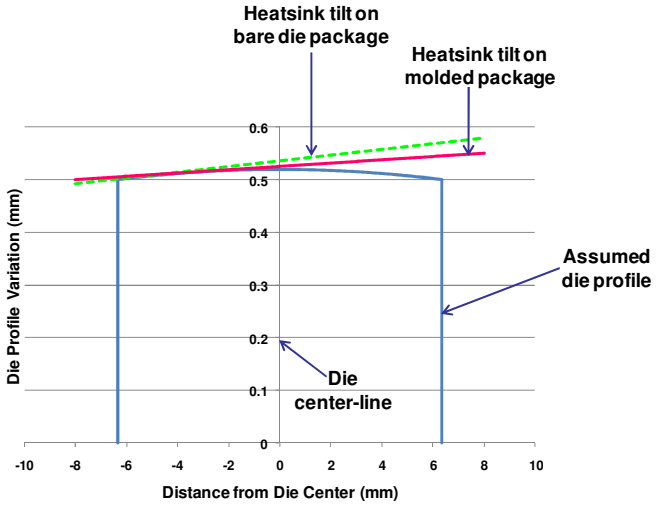


Figure 17: 2-D analysis of package tilt under non-uniform loading

A zoomed image of the assumed profile is depicted below in Figure 18 to clarify the point in discussion.

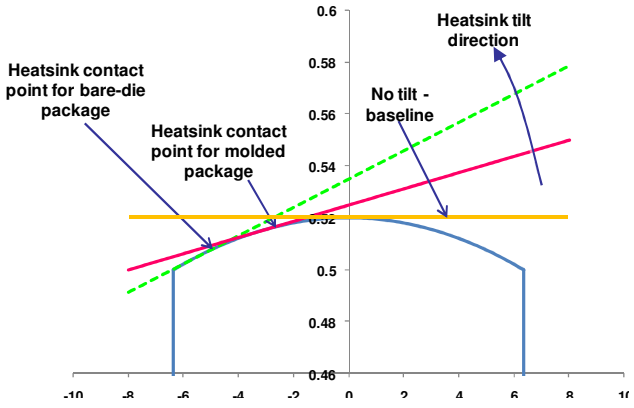


Figure 18: Package tilt analysis

The curved surface of the warped die profile was assumed to be parabolic and is represented by the below equation:

$$y = t_{die} - \frac{\alpha x^2}{(L_{die})^2} \tag{3}$$

where, t_{die} is the total die thickness = 0.52 mm, L_{die} is the die length, α is a constant.

The slope of the tangent to the parabola m, at any given point (x_1, y_1) is given by:

$$m = \left.\frac{dy}{dx}\right|_{(x1,y1)} = -\frac{2\alpha x_1}{(L_{die})^2} \tag{4}$$

The equation to the tangent to the parabola at a given point (x_1, y_1) is given by:

$$(y - y_1) = -\frac{2\alpha x_1}{(L_{die})^2}(x - x_1) \tag{5}$$

The average TIM-II BLT can be estimated by calculating area between the heatsink base and the die warped profile and dividing it by the die length as shown in the below equation:

$$Average\ TIM - II\ BLT\ = \frac{\int_{-L_{die}/2}^{+L_{die}/2} [(y_1 - \frac{2\alpha x_1}{(L_{die})^2}(x - x_1)) - (t_{die} - \frac{\alpha x^2}{(L_{die})^2})]\, dx}{L_{die}} = \frac{\alpha x_1^2}{{L_{die}}^2} + \frac{\alpha}{12} \tag{6}$$

As seen from equation 6 above, the average TIM-II BLT is directly proportional to the square of the x-coordinate of where the heatsink contacts the die. Therefore, since the heatsink in the bare die package would contact the die at point further away from the die-center as compared to the molded package; this would in turn result in a greater average TIM-II BLT for the bare-die package as compared to the molded package. This would increase the TIM-II thermal resistance as shown in equation 1. Similar analysis can be performed to show that lidded package would achieve lower TIM-II BLT in comparison to the molded package. The effective TIM-II area for thermal dissipation will also be greater for the lidded package due to the thermal spreading in the heat-spreader. This in turn would lower the effective TIM-II resistance as well.

One can also perform a worst case analysis (wherein the heatsink barely contacts the edge of the die) to estimate the maximum average TIM-II BLT for both the bare die and molded packages using the above model. For bare die package, the worst case scenario would represent the case wherein the heatsink contacts the substrate perimeter top edge and the die perimeter top edge. This would result in an average TIM-II BLT of about ~333 µm. For molded package, the worst case scenario would represent the case wherein the heatsink contacts the mold perimeter top edge and the die perimeter top edge. This would result in an average TIM-II BLT of about ~21 µm assuming that the mold surface is flat and 50 µm below the die surface.

Summary & Conclusions

The primary goal of the paper is understand the impact of non-uniform loading on package thermal resistance and to provide a merit analysis of package designs as a function of thermal performance. As seen from the results, the molded package is tilt-resistant in comparison to the bare die package and helps in achieving a better thermal performance. Work is in progress on performing the measurements on factory assembled molded and lidded packages with a larger sample size (~30 per leg) in order to present statistically significant data.

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