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Overview

The goal of IEEE P1687 Internal JTAG (IJTAG) is to streamline the use of instruments that have been embedded in chips. The intent is to facilitate the deployment of these embedded instruments in a wider array of chip, board and system level validation, test and debug applications. Over the last decade, semiconductor manufacturers have embedded instruments in their chips to simplify the characterization, testing and debugging of these devices. Given the right standards-based tools environment, these same instruments can perform a much broader spectrum of chip, board and system level validation, test and debug applications.

Industry Drivers

Several conditions in the electronics industry are motivating this trend toward embedded instrumentation and thereby have created a need for the IEEE P1687 IJTAG standard. For circuit boards, the progress of advanced technologies such as complex microprocessors and very high-speed buses has outstripped the capabilities of the older legacy validation and test equipment. By and large, this legacy equipment is intrusive in that it is external to the board being tested and it relies upon placing a physical probe on some sort of an access point on the board or on a chip on the board. For a number of reasons, the effective availability of these access points is rapidly diminishing and this is reducing the validation and test coverage that can be achieved with legacy intrusive testers, such as oscilloscopes and logic analyzers for validation, and in-circuit test (ICT) and manufacturing defect analyzers (MDA) for production test. Because the testing of boards with external, intrusive instrumentation has become increasingly less effective, the industry has turned to non-intrusive software-based embedded instrumentation which executes out of hardware on the board being test and is not limited by physical probes.

At the chip level, there are several other factors that are driving the industry toward embedded instrumentation. Keeping pace with Moore’s Law has meant that chips have become much denser in terms of the number of transistors per square millimeter. In addition, chip frequencies have gone up significantly and devices are much more complex. All of this means that characterization times are longer and more sophisticated test equipment is needed. Advanced chip packaging concepts such as stacking multiple die in three-dimensional packages also complicates chip-level characterization and debug.

The time-to-market for electronic products is rapidly shrinking and this affects all aspects of a product’s development cycle, including validation and test. For example, the average life of a cell phone today is approximately eight months. In the past, test routines were developed separately for each phase of product development and manufacturing. Now, the industry cannot afford the luxury of the extra time that is needed to re-develop tests for a product as it transitions from each phase in its life. Portable tests and other routines that accompany chips and which can be re-applied in every phase of a product’s life cycle are becoming a necessity because of the shorter life cycles. To achieve this level of portability the tests must capitalize on embedded instrumentation. One way to do so will be the capabilities of the IEEE P1687 IJTAG standard.
The Synergy of Standards

To fully capitalize on embedded instrumentation, several other standards besides the IEEE P1687 IJTAG standard often work together. These would include the IEEE 1149.1 Boundary-Scan Standard and its enhanced version, the IEEE 1149.7 Enhanced Boundary-Scan Standard, as well as the IEEE 1500 Core Test Standard.

Who will use IEEE P1687 IJTAG?

The IEEE P1687 IJTAG standard will be applied at the chip and board levels. Chip designers, for example, will find IJTAG useful during design verification when it will be used in conjunction with a simulator or emulator. IJTAG will also be deployed in the ATE test environment where it will become part of chip test, chip debug/diagnostics and chip characterization.

At the circuit board level, the IEEE P1687 IJTAG standard will be used to access instruments that are embedded in chips to perform board-level test, debug/diagnostics and characterization.

Finally, when a system is failing in the field, maintenance personnel can utilize the same tests based on embedded instruments to extract failure data from a device. This data, along with other environmental data, such as voltage and temperature, can be fed back to the organization’s failure analysis team which can analyze the root causes of failures. This will allow the duplication of the failure conditions and as a consequence reducing reduction in the amount of No Trouble Found (NTF) cases.
The Basic P1687 On-Chip Architecture

Figure 1: The Basic IEEE P1687 IJTAG Architecture

The figure above illustrates the architecture that the IEEE P1687 IJTAG standard would implement at the chip level. On the right, it shows how the IJTAG network interfaces to the IJTAG-compliant embedded instruments with the IEEE 1149.1 boundary-scan standard’s Test Access Port (TAP) on the left. The TAP functions as the interface for the embedded P1687 IJTAG architecture to the world outside of the chip.

Essentially, IEEE P1687 IJTAG allows the boundary-scan TAP and its TAP Controller to access instruments that are embedded on-chip. Several IJTAG concepts are shown in this illustration, including the Segment Insertion Bit (SIB) and Procedural Description Language (PDL). These will be described at greater length below.
The Instrument Gateway (Interface)

The above drawing illustrates how the hardware interface or gateway for the IEEE P1687 IJTAG standard on-chip architecture can interface to a standard IEEE 1149.1 boundary-scan standard Test Data Register (TDR). Isolating the P1687 IJTAG architecture from the requirements of the interface leading off the chip ensures the portability of embedded instrument intellectual property (IP) as well as any vector IP that may be associated with them. In fact, an off-chip interface other than the IEEE 1149.1 boundary-scan TDR could emerge in the future and this would not affect the portability of IEEE P1687 IJTAG instruments or vectors.
Managing 1687 scan paths with the Segment Insertion Bit (SIB)

The Gateway Segment-Insertion-Bit (SIB)

The Key Element for Adding, Organizing, Managing Embedded Content

One of the key elements defined in the IEEE P1687 IJTAG standard is the Segment Insertion Bit (SIB). The composition of a SIB is shown in the illustration above. A SIB is similar to an IEEE 1149.1 boundary-scan shift/update cell, but the SIB is used to dynamically configure an on-chip P1687 IJTAG scan path to meet the requirements of a particular set of test vectors. ‘Selecting’ a certain SIB can activate a portion of the chip’s IJTAG scan path and consequently activate the instrument(s) on that segment of the scan path. Conversely, ‘de-selecting’ a SIB will deactivate a portion of the chip’s overall scan path and render the instruments on that segment inaccessible. Instruments on a deactivated segment of the scan path cannot be accessed as long as the scan path segment is deactivated, but they can still execute test vectors while they are offline.

IJTAG Description Languages

There are two description languages defined by the IEEE P1687 IJTAG standard: Instrument Connectivity Language (ICL) and Procedural Description Language (PDL).
ICL describes the IEEE P1687 hardware architecture that is implemented on a chip. Essentially, it describes the scan paths and the instruction registers that are associated with each scan path. Since an IEEE P1687 SIB can activate or deactivate segments of a chip’s total scan path, any number of different scan paths can be implemented on a particular chip. ICL is used to describe each of these scan paths.

PDL defines the instrument’s operations and functions and it is eventually turned into test vectors that are associated with each IEEE P1687 IJTAG instrument that is embedded on a device. In addition, PDL will document each instrument’s actions and sequences.

The IJTAG Network Building Block

Figure 4: The simplest IEEE P1687 IJTAG Network

The drawing above illustrates the most basic unit or building block in an IEEE P1687 IJTAG architecture. Shown here as a block diagram is an IEEE 1149.1 boundary-scan standard’s TAP controller on the left, which provides access from the outside world to the on-chip IJTAG architecture. The TAP’s Test Data In (TDI) and Test Data Out (TDO) registers are connected in a scan path to a boundary-scan Test Data Register (TDR) which acts as a read/write front-end to an IEEE P1687 IJTAG embedded instrument. As noted in the drawing, IJTAG’s ICL language defines the read/write signals that interface the TDR to the embedded instrument. And IJTAG’s PDL defines the actions, test vectors and other operations that the instrument executes.
Conclusion

This is very brief overview tutorial of the IEEE P1687 IJTAG embedded instrumentation standard. It is by no means comprehensive. An expanded version of this tutorial will be forthcoming from ASSET as the standard nears ratification.

For further information on the IEEE P1687 IJTAG standard visit the working group’s web site at http://grouper.ieee.org/groups/1687/.