

# Bonding Technologies for 3D Integration

An overview about different interconnects used during the system evaluation of the FINEPLACER® sigma

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## Abstract:

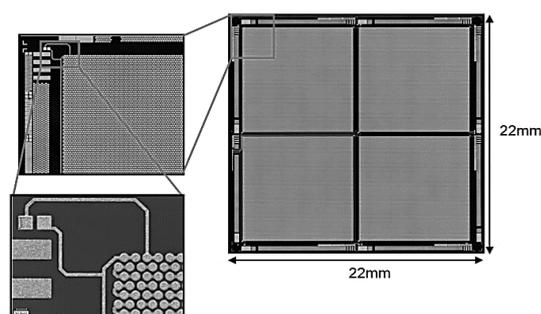
Tougher requirements related to the request for smaller, lighter and multi-functional electronic devices impose increased demands on IC packaging. Ever more complex circuitry, fine pitch and micro bump designs and die stacking are examples of how the industry meets these demands. Finding a suitable process technology for 3D packaging can be a challenge. This paper provides information about various connection methods predominantly used in today's 3D packaging. In comprehensive trials, various dies characterized by high bump count (up to 143,000), fine pitch (down to 25  $\mu\text{m}$ ) and small bump diameter (down to 13  $\mu\text{m}$ ) were placed on a substrate using a FINEPLACER® sigma bonder. This whitepaper describes test procedures for different 3D integration technologies and presents utilized process parameters and results.

Keywords: 3D packaging, transient liquid phase bonding, metal-diffusion-bonding, Cu-Cu thermo compression, eutectic bonding, high bump count

## Introduction

Higher speed, higher density, optimized size and multifunctionality are the main drivers in the evolution of electronic devices. 3D stacked structures are important to meet future demands especially of microprocessors, memory components, image sensors or IR sensors.<sup>[1]</sup>

A proper interconnection technology depends on various requirements, such as small form factor, small pitch, thermal, electrical and mechanical stability. These can be fulfilled by Metal Diffusion (MD) Bonding or Transient Liquid Phase Bonding (TLPB). In order to handle a high bump count, small pitch and low standoff height, a precision flip-chip bonder capable of high placement accuracy, high bond force and co-planar placement is mandatory.



Pic. 1: Layout of the substrate (IZM-ASSID)

In order to get meaningful results, various chip designs and associated interconnection technologies (as shown in table 1) were used during the trials. The overhang of 1 mm between substrate and top die on each side is used to apply probe needles. After bonding, the electrical contact of the daisy chain can be verified. An electrical pass can be measured only, if every bump has proper contact.

The challenge was to place or bond the chips with a force of up to 500 N and a heating plate temperature of more than 300 °C while ensuring post-bond accuracy of less than 3  $\mu\text{m}$ .

The results were determined based on a number of analytical methods, such as x-ray, electrical tests and cross-sections.

Chip size	Bump diameter Bump count	Bonding technology
10x10 mm <sup>2</sup>	Bump $\varnothing$ 25 $\mu\text{m}$ 35,904	TC Bonding with NCF
10x10 mm <sup>2</sup>	Bump $\varnothing$ 25 $\mu\text{m}$ 35,904	TLPB/ SLID Bonding
11x11 mm <sup>2</sup>	Bump $\varnothing$ 13 $\mu\text{m}$ 13,312	Thermo Compression Bonding
20x20 mm <sup>2</sup>	Bump $\varnothing$ 25 $\mu\text{m}$ 143,616	Eutectic Bonding

Table 1: The different chip designs used for the evaluation

## Thermo compression with pre-underfiller

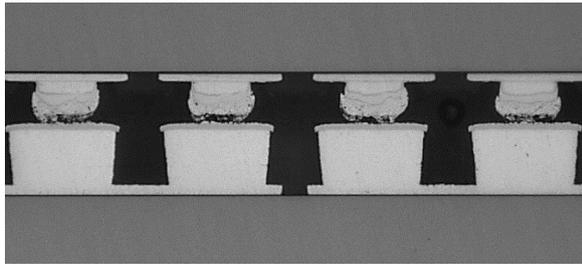
Underfilling very thin (< 100  $\mu\text{m}$ ) or stacked dies is not trivial because adjacent components or surrounding structures can easily be contaminated. Therefore, pre-underfillers have become increasingly popular.<sup>[2]</sup> Those underfillers will be applied on die or substrate before bonding. During the final mounting process the material begins to flow, filling the space between the bumps and becomes cross linked.

Non Conductive Foils (NCF) is a version of pre-underfiller, applied to the wafer via vacuum laminator before dicing. During the bonding process, a specific force and temperature is needed to liquefy and subsequently activate the underfill material.<sup>[3]</sup>

The top die was placed onto the substrate at room temperature and heated slowly up to 120 °C so that the viscosity of the NCF lowers.

Resulting from that, the material will be displaced by the bumps. At 120 °C the NCF starts to cross-link, therefore the bumps have to be in contact. During this process step the applied force is highly crucial as it should always be above 1 g per bump. Subsequently, the package was heated up to the final temperature of 231 °C.

The post bond accuracy of the package was below 2 μm, even with a 500 N bond force and a bonding temperature of more than 230 °C.



Pic. 2: cross section of test chip 2 with NCF bonded with 500 N

For pre-underfilled chips with a low bump height, coplanarity is crucial. For this process a gimbal-style placement tool was used to allow self-levelling of the chip before and during bonding. The result was checked via cross section and indicated an average parallelism error of just 2 μm over the length of 15 mm.

For this technology, a highly optimized process and perfect timing are crucial. If temperature and force ramps do not match 100%, the bond result will be influenced dramatically. For example, if the force is applied too late the bumps won't be in contact completely.

#### Solid Liquid Interdiffusion Bonding (SLID)

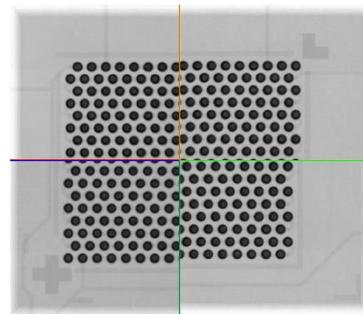
SLID becomes increasingly important especially in multi-chip assembly or 3D-integration due to its beneficial characteristics which it owes to the physical properties of diffusion. A low-fusing solder layer between two high-fusing metals is heated to its melting temperature. This generates an inter-metallic compound based on diffusion with a melting point higher than the melting point of the low-fusing solder. This technology is also known as Transient Liquid Phase Bonding (TLPB), and has its benefits especially in Cu-Sn systems.<sup>[1]</sup>

During the trials the chips were initially connected with a force of 20 N and then bonded with a 500 N bond force once the melting point of 231 °C was reached.

In order to ensure a uniform inter-metallic compound, an oxide-free bond layer is of utmost importance. The existing test chips were cleaned in plasma prior to bonding. In addition, flux was used during the bonding process.

To avoid lateral drift due to the spherical surface of the chip's and substrate's solder bumps, the final force application had to be conducted with the solder in liquid state. To generate an inter-metallic phase, the assembly had to be stored at 200 °C from several minutes to a couple of hours.

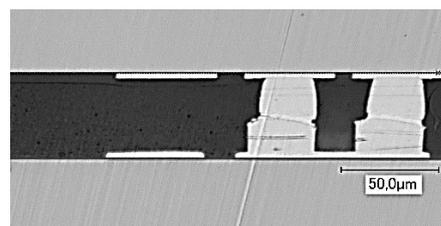
Subsequent tests via x-ray and cross-section images proved good results.



Pic. 3: The x-ray of the 4 corners indicates a centric assembly

Despite high forces and spherical surfaces, a post bond accuracy of 3 μm was reached. The result can partly be attributed to the specific chip layout since the fiducials and bumps had been applied in two separate lithographic processes. Based on the statements made by the chip manufacturer, a potential offset of up to 5 μm has to be taken into account.

Due to the spherical surfaces, coplanarity is particularly dependent on the placement accuracy. Even minor angular errors may result in bumps being pushed aside due to the high bond forces.



Pic. 4: bump deformation due to lateral forces

An electrical contact could be measured along the entire daisy chain on every bonded sample which indicates a robust bonding technology.

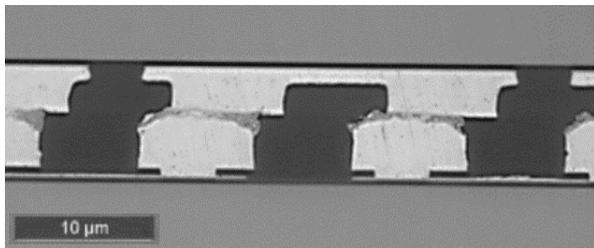
#### Thermo Compression Bonding

Metal-to-Metal Bonding is very interesting for chip packaging and especially image sensors due to the "mainstream" material that is copper. High electrical and thermal conductivity are main advantages of this material. Via Cu-Cu-Thermo-Compression-Bonding, it is possible to also benefit from these advantages when it comes to the interconnection of chip and substrate.<sup>[4]</sup>

In order to improve the bond process, a thin SnAg layer of 1µm was plated onto the bumps of the top die. This effect has already been verified during former studies.<sup>[3]</sup>

For the 13,312 contacts with a diameter of 13 µm and a pitch of 25 µm, a force of 500 N and a temperature of 300 °C is required. To ensure proper contact it is necessary to remove oxide on the chips and substrates via plasma before bonding. The annealing process at 400 °C was skipped for these initial tests.

Due to the small bump diameter and the small pitch, the placement accuracy could be checked via cross section only and displays a post-bond accuracy of 1-3 µm. To improve those results it is necessary to adapt the process parameters such as temperature and force.



**Pic. 5:** example of lateral shifting in bond process

The parallelism error measured on the diagonal of that 11 mm x 11 mm was 2 µm. Related to those results the electrical test showed proper electrical contact without any short for every daisy chain on this chip.

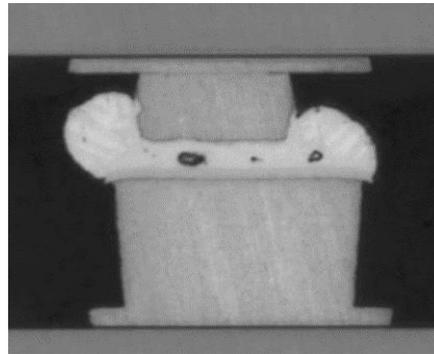
#### **Eutectic Bonding**

Eutectic Bonding is still a very common and extensively tested technology with a eutectic alloy as contact medium. Usually the single chips will be stacked and soldered at one via reflow or contact heating from bottom only. Due to accuracy requirements it is important to perform every single process step in one system without any additional substrate handling process. For this test a single chip with 143,616 bumps was placed and held in position during the whole process.

The used SnAg alloy with 3.7 % Ag-amount has a melting temperature of 221 °C which needs to be exceeded during the bonding process. <sup>[3]</sup>

For precise alignment, the chips were placed at room temperature and heated up to the melting temperature by using a defined profile. To ensure a proper contact, the chip was held in position with a force of 20 N, but in this case the self-alignment effect is not possible.

With this technology it was possible to bond this large chip with a parallelism error of 1.7 µm over a length of 28.3 mm and 2-3 µm accuracy. One disadvantage of this technology is the increased void generation inside the alloy. Alternately, this process has to be done under vacuum.



**Pic. 6:** bond result with small voids

#### **Conclusion**

New bonding methods like Metal Diffusion Bonding, Direct Metal to Metal Bonding as well as pre-underfilled chips are very demanding in terms of accuracy and process parameters. Forces up to 1000 N, a bond temperature up to 400 °C and a requested post bond accuracy of 1-3 µm impose high requirements on material and equipment.

With the FINEPLACER® sigma it was possible to bond even highly sophisticated chips with high bump count, small diameter and pitch very accurately, so that proper electrical contact could be established on all bumps (more than 143,000). The integrated process management software allows optimization of all parameters for a good and reliable bond result.

#### **References**

- [1] Process-dependent Microstructure Changes in Solid-Liquid Interdiffusion Interconnects for 3D Integration (English); Iuliana Panchenko (Autor); Detert, M (2014); ISBN-10: 3934142656
- [2] SiP Global Summit; Underfill design and trend for 2.5D/3D with TSV package; Haruyuki Yoshii; 2013
- [3] Engineering report; System Evaluation of FINEPLACER sigma; Ref. 20150227; Alexander Wollanke; IZM-ASSID; 2015
- [4] Enabling Cu-Cu Thermocompression Bonding for MEMS via Au Capping Layer; David Borowsky; IMS Chips, Stuttgart, Germany