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White Paper

Uprating of Ceramic Capacitors

By Craig Hillman, PhD

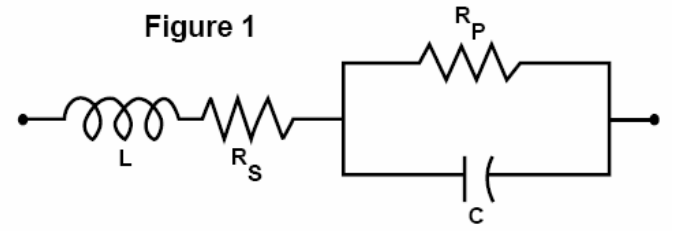
5110 Roanoke Place, Suite 101 College Park, Maryland 20740
Phone (301) 474-0607 Fax (240) 757-0053
www.DfRSolutions.com

Uprating of Ceramic Capacitors

Ceramic capacitors are chip components that consist of alternating layers of dielectric material and metal conductors (typically AgPd or Ni alloys). Ceramic capacitors are primarily used to filter high-frequency electrical signals and because of their extremely high capacitance-to-volume (C/V) values.

The critical functional parameters of ceramic capacitors are defined as capacitance (C), equivalent series resistance (ESR), insulation resistance (IR), and dissipation factor (DF). These parameters are interrelated through the following schematic

Figure 1



where Rp is insulation resistance and Rs is ESR. As with electrolytic capacitors, insulation resistance, and therefore leakage current, is driven primarily by the behavior of the dielectric. Insulation resistance is relatively high for ceramic capacitors, with resulting negligible leakage current. ESR is primarily driven by the behavior of the electrolyte. Physically, impedance (Z) is a summation of all the resistances throughout the capacitor, including resistances due to packaging. Electrically, Z is the summation of ESR and either the capacitive reactance (X_C), at low frequency, or the inductance (L_{ESL}), at high frequency (see **Error! Reference source not found.**). Dissipation factor is the ratio of ESR over X_C. Therefore, a low ESR tends to give a low impedance and a low dissipation factor.

1. Functional Parameters (Specified in Datasheet)

An example of the variation in functional parameters that can be provided in manufacturers' datasheets is listed below

Manuf.	EPCOS	TDK	MuRata	MuRata	Taiyo Yuden	Taiyo Yuden
Part	B37944	Fixed, Class 2	GRM21BF5	GRM32CF5	LMK	TMK
Temp.	-30 to 85C	-30 to 85C	-30 to 85C	-30 to 85C	-30 to 85C	-30 to 85C
C	+22% / -82%	+22% / -82%	+22% / -82%	+22% / -82%	+22% / -82%	+22% / -82%
IR	> 10^4 M□ @ 20C	> 500 M□	> 227 M□	N/A	> 10^4 M□ @ 20C	> 10^4 M□ @ 20C
DF	0.125 at 20C	0.05 at 20C	0.09 at 20C	0.20 at 20C	0.16 at 20C	0.035 at 20C

1.1 *Capacitance vs. Temperature*

Class II dielectrics are well known to have capacitance values that can be very sensitive to temperature (see Figure 3). Since Y5V is an EIA performance specification and does not define a particular mixture, the capacitance behavior over the given temperature range can vary extensively while still staying within the requirements of +22% / -82%. Some of the capacitance behaviors displayed in Figure 1 through Figure 3 suggest that Y5V capacitors could drop below -82% when temperatures reach -40C.

However, once any significant bias is applied to these capacitors, the actual capacitance drops precipitously and the capacitance change over temperature is minimized (see Figure 4).

1.2 *Insulation Resistance vs. Temperature*

As a general statement, insulation resistance logarithmically decreases with increasing temperature (see Figure 5 and Figure 6). There is some variation on how manufacturers specify insulation resistance.

TDK and MuRata do not state a specified temperature for their insulation resistance value. Therefore, the value provided in their datasheets can be interpreted that the manufacturer guarantees this maximum leakage current over the specified temperature range. This may also explain why their insulation resistance values are lower than Epcos, which clearly indicates an insulation resistance value at 20C, and Taiyo Yuden, which indicates that all testing is performed under "standard test conditions".

While Epcos and Taiyo Yuden's failure to provide insulation resistance over the specified temperature range does provide some risk, review of test results from the literature seem to indicate that a decrease in insulation resistance greater than one order of magnitude from room temperature to 85C is unlikely. This would still provide 100 M□ of resistance, which should be sufficient for most applications. In addition, EIA specifications require that the RxC product exceed 1000 Ohm-Farad (often expressed as 1000 Megohm-Microfarad) at 25°C, and 100 Ohm-Farad at 125°C, (10% of the values of Table G-1 (see Figure 7)).

1.3 *ESR vs. Temperature*

Manufacturers of ceramic capacitors do not provide an ESR value in their datasheet nor do they specify the maximum variation in ESR over the specified temperature range. While this could be somewhat discerning, the ESR values of ceramic capacitors are typically very low (ceramic capacitors are often selected in applications requiring low ESR).

However, the behavior of the dissipation factor, which is directly influenced by ESR, as a function of temperature is provided.

1.4 *Dissipation Factor vs. Temperature*

The complexity of the ceramic microstructure and the resultant multiple Curie Points of the aggregate polycrystalline components in any given formulation do not permit a clear prediction of DF behavior with temperature, other than the fact that DF is inversely proportional to temperature. At elevated temperatures below the Curie Point, DF is relatively stable. However, at cold temperatures, especially below 0C, the dissipation factor can increase by a factor of 5 above the manufacturer's specifications (see Figure 8 and Figure 9).

However, as with capacitance, this significant increase is minimized once any significant bias is applied.

2. Functional Parameters (Not Specified in Datasheet)

All functional parameters are specified within the manufacturer's datasheet

3. Electrical Overstress[1] (Robustness)

Ceramic capacitors can experience electrical overstress type failure mechanisms through the application of excessive voltage or excessive current.

3.1 Voltage Rating

The capacitor manufacturers do not provide any indication on the variation on breakdown strength as a function of temperature. However, two activities by the manufacturer tend to limit any concern about change in the voltage rating. First, a standard screen in the industry is to apply a 2X rated voltage. Second, the industry standard life tests require testing at 2X rated voltage and maximum rated temperature for 1000 to 2000 hours. Therefore, the design of the capacitor has been demonstrated to be robust to dielectric breakdown to the extremes of the manufacturer's ratings.

3.2 Current or Power Rating

Ceramic capacitors can experience a temperature rise due to the application of elevated levels current or power. Capacitor manufacturers often provide recommended limits on current or power to prevent temperature rises greater than 20C or temperatures greater than the specified maximum temperature. Review of existing datasheets found minimal information on this need for derating outside of MuRata and Syfer (see Figure 10 and Figure 11).

4. Wearout Behavior

The wearout behavior of ceramic capacitors, degradation in insulation resistance due to migration of vacancies, is well known and is captured by the industry standard wearout model

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\frac{E_a}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

where t is time, V is voltage, T is temperature (K), n is a constant (1.5 to 7), E_a is an activation energy (1.3 to 1.5) and K_B is Boltzman's constant (8.62 x 10-5 eV/K). Wearout of ceramic capacitors has typically not been an issue, but increasing miniaturization has resulted in capacitor materials and architectures that could wearout within 10 years (see Figure 12). This behavior is dependent upon the capacitance/volume ratio (C/V).

The C/V ratio of concern is approximately greater than 5 to 10 uF/mm3. This equates to roughly 2 to 3 microns of dielectric thickness. Unfortunately, most customers of ceramic capacitors often are unaware of the component thickness, which prevents a calculation of C/V. Therefore, an alternate approach is to list capacitance levels of

[1] Mechanical overstress mechanisms are relatively independent of temperature

concern for a given case size and dielectric material. One example is X5R in an 0805 case size. Reliability assessments should be performed once capacitance levels are 10 uF or higher.

Capacitors are also known to 'age', which induces a drop in capacitance over time (see Figure 13). Y5V dielectric ages approximately 5-7% per decade. Quantitative information about the change in aging rate as a function of temperature were not obtained, but it is believed to be relatively temperature independent, with the driving force for aging reducing with increasing temperatures.

5. Conclusion

The primary risk in using ceramic capacitors beyond their rated temperatures is the potential for insufficient reliability of ceramic capacitors with extended value (high C/V ratios).

Figures

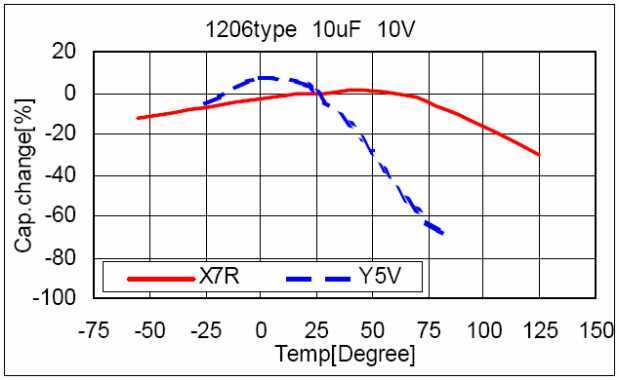


Figure 1: Change in capacitance as a function of temperature for Y5V dielectric ceramic capacitors in general (left) and GRM21BF51H105ZA12L specifically (right)[MuRata]

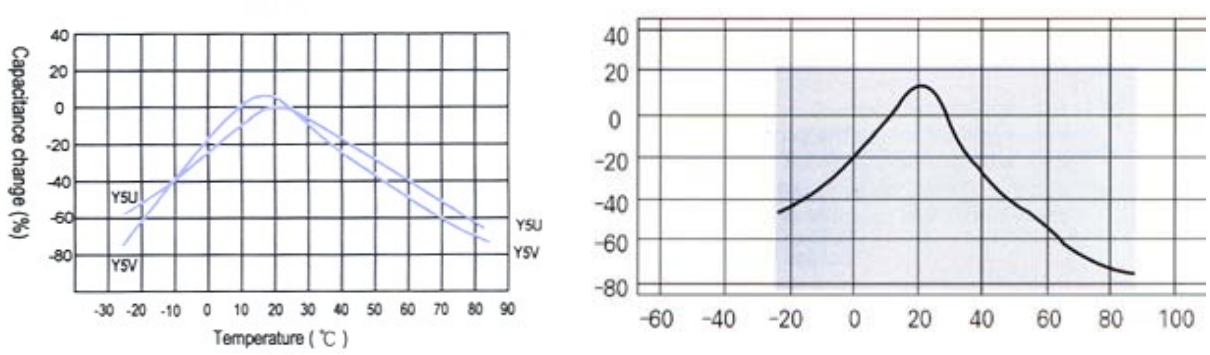


Figure 2: Change in capacitance as a function of temperature for Y5V dielectric ceramic capacitors (left: Supertech Electronic; right: CEC International)

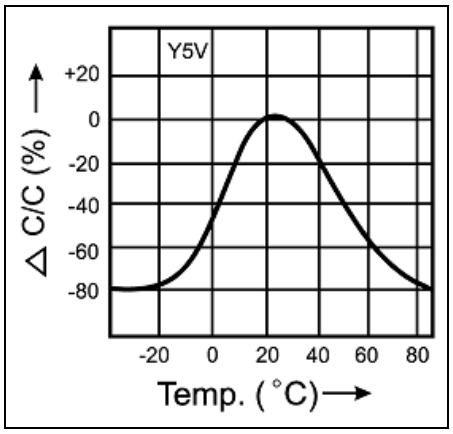


Figure 3: Change in capacitance as a function of temperature for Y5V dielectric ceramic capacitors (Ease Electronics)

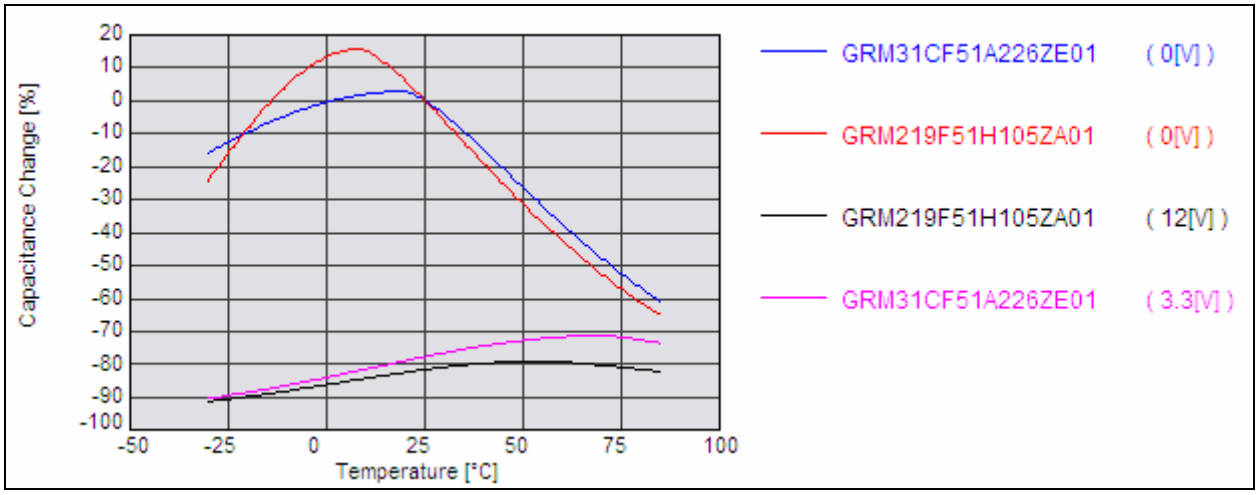


Figure 4: Change in capacitance as a function of temperature for Y5V dielectric ceramic capacitors with an applied bias

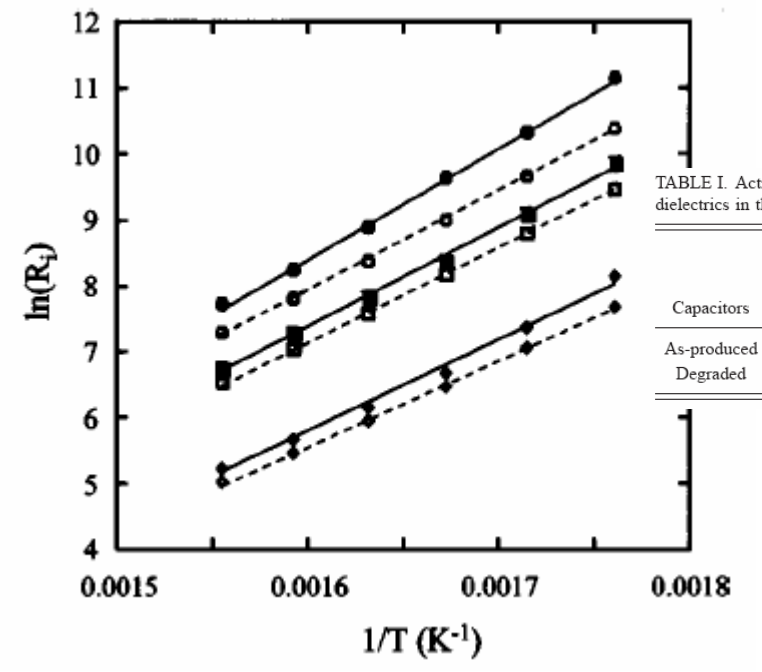


TABLE I. Activation energies of electrode interfaces, grain boundaries, and dielectrics in the as-produced and degraded MLCCs.

	E_A (eV)		
Capacitors	Electrode interfaces	Grain boundaries	Grains
As-produced	1.45±0.02	1.30±0.02	1.21±0.03
Degraded	1.29±0.01	1.23±0.01	1.11±0.02

Figure 5: Change in the components of insulation resistance (electrode, grain boundaries, and grains) as a function of temperature[2]

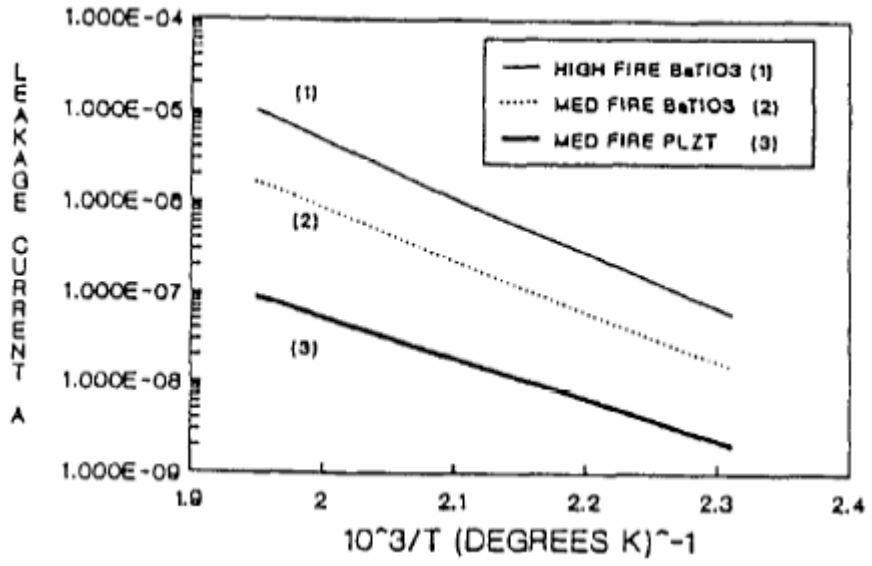


Figure 6: Change in leakage current as a function of temperature[3]

[2] JOURNAL OF APPLIED PHYSICS VOLUME 96, NUMBER 12 15 DECEMBER 2004, Oxygen nonstoichiometry and dielectric evolution of BaTiO3. Part II—insulation resistance degradation under applied dc bias, G. Y. Yang, et. al.
[3] A ceramic capacitor for AC applications, Burks, D.; Hofmaier, R.; Knudtsen, S.; Shirn, G., Electronic Components Conference, 1989. Proceedings., 39th, Date: 22-24 May 1989, Pages: 194 - 201

TABLE G-1
MINIMUM IR STANDARDS VS. CAPACITANCE

Capacitance	Min IR (GΩ)	Min RxC (ΩF) @ 25°C
0.1 pF to .010 µF	100.00	1000
.015	66.67	
.022	45.45	
.033	30.30	
.047	21.28	
.068	14.71	
.100	10.00	
.150	6.67	
.220	4.55	
.330	3.03	
.470	2.13	
.680	1.47	
1.00	1.00	
etc.	etc.	

Figure 7: Minimum IR standards vs. capacitance as per EIA specifications

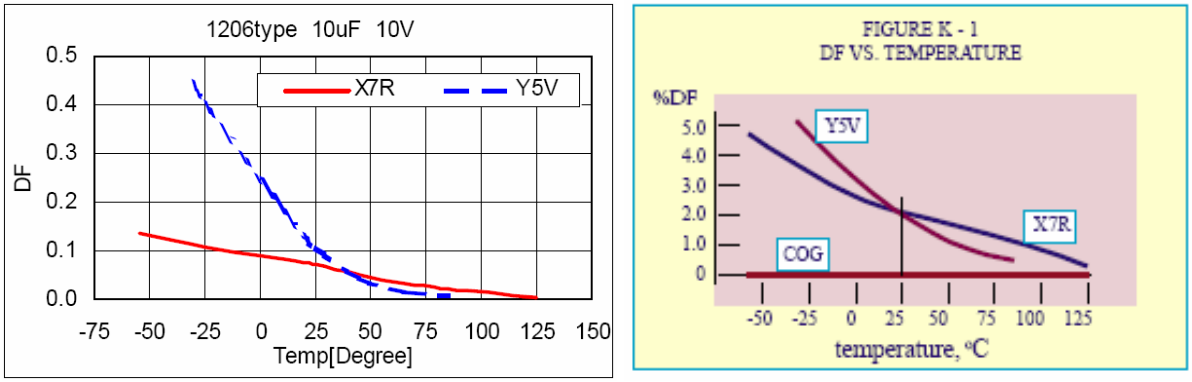


Figure 8: Change in dissipation factor as a function of temperature for Y5V dielectric ceramic capacitors (left: MuRata; right: Novacap)

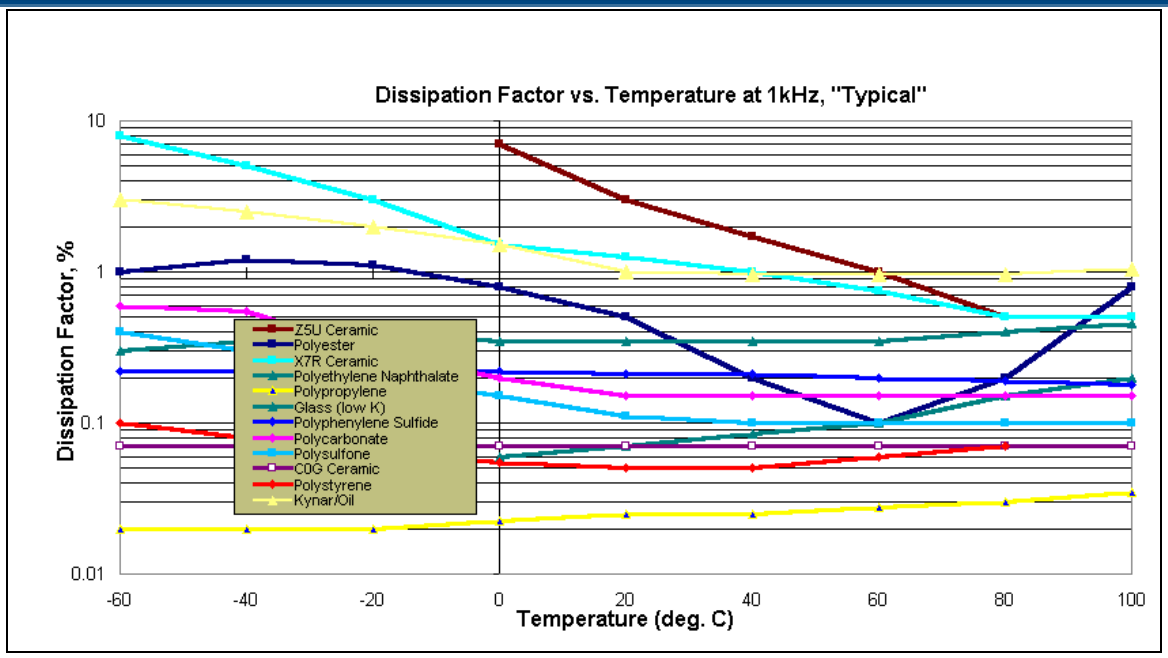


Figure 9: Change in dissipation factor as a function of temperature for capacitors (http://my.execpc.com/~endlr/DF_VS_T2.GIF)

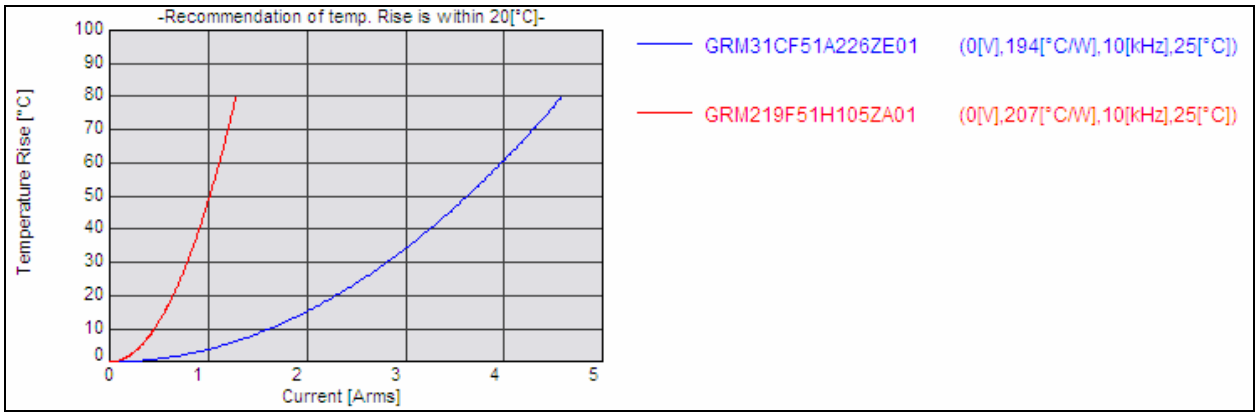


Figure 10: Temperature rise as a function of applied current for Y5V dielectric ceramic capacitors (Murata)

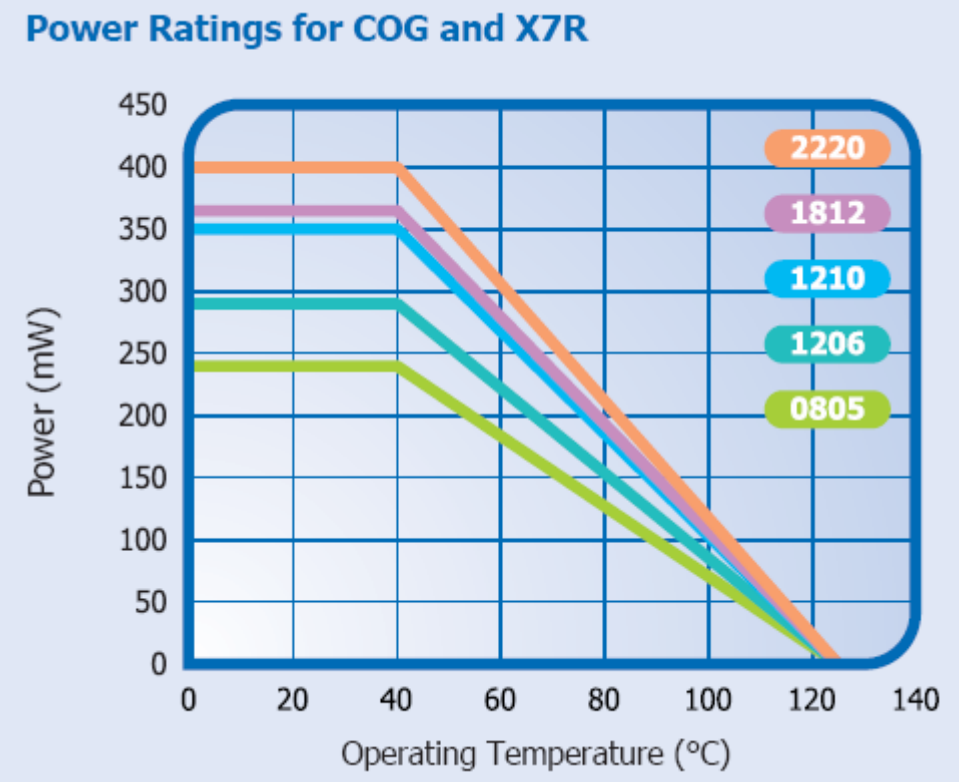


Figure 11: Power derating curves for C0G and X7R dielectric ceramic capacitors as provided by Syfer

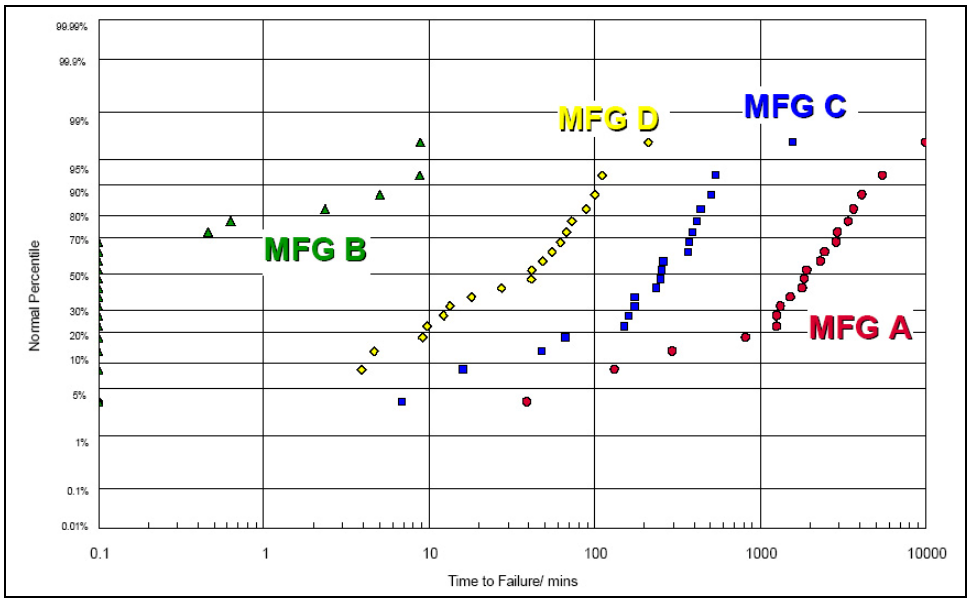


Figure 12: Time to failure under elevated voltage and temperature conditions (Kemet). Extrapolation using the industry standard formula finds time to 1% failure of less than 10 years with 50% rated voltage and an ambient temperature of 45C

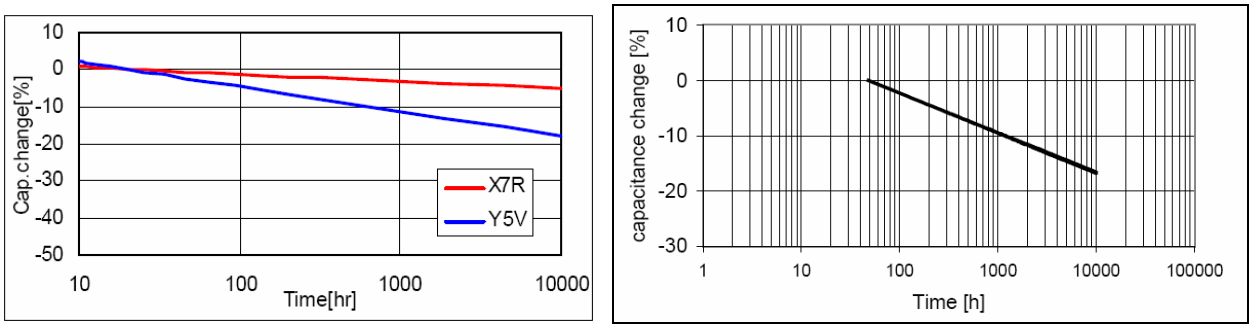


Figure 13: Change in capacitance over time for Y5V dielectric ceramic capacitors (left: MuRata; right: Epcos)

Type	Model	Temperature characteristics	Rated voltage	Electrostatic capacity
0603	GRM03	C△	25V	0.5pF~100pF
		B	16V	100pF~1000pF
			10V	1500pF~0.1μF
			6.3V	15000pF~0.1μF (0.22μF)
		F	10V	2200pF~10000pF
1005	GRM15	C△	50V	0.5pF~1000pF
		B	50V	220pF~4700pF
			25V	4700pF~47000pF
			16V	47000pF~0.1μF
			10V	0.1μF~1.0μF
			6.3V	0.33μF~1.0μF (2.2μF)
		F	50V	2200pF~10000pF
			25V	22000pF~0.1μF
			16V	47000pF~0.47μF
			10V	0.22μF~1.0μF
			6.3V	1.0μF

Figure 14: Capacitance capability from Murata based on dielectric, case size, and rated voltage (0603 is 0.6 mm x 0.3 mm and 1005 is 1 mm x 0.05 mm)