XJTAG adds support for Xilinx Virtex-5 FPGA System Monitor

- Xilinx System Monitor complements XJTAG’s extensive debug and test capability by providing on-chip power supply monitoring, temperature monitoring, and precision analogue inputs

CAMBRIDGE, England, May 15, 2007 – XJTAG, a leading supplier of IEEE Std. 1149.1 compliant boundary scan tools, has enhanced its development system by adding support for Xilinx’s recently announced new feature, the Virtex-5 FPGA System Monitor. This will provide XJTAG users with easy access to what is the industry’s first FPGA analogue debug and system management tool for thermal management and measurement of on-chip power supply voltages.

“These new features complement our already extensive debug and test capabilities by allowing customers to check power supplies or perform overall thermal management using the JTAG port on the 65-nm Virtex-5 FPGAs,” said Dominic Plunkett, chief technology officer at XJTAG.

The Xilinx System Monitor is built around a fully specified 10-bit 200kSPS (kilo-Sample-Per-Second) general purpose analogue-to-digital converter (ADC). Automatic calibration and self check features ensure accurate and reliable measurements over a temperature range of -40C to +125C.

The System Monitor is now fully integrated within the XJTAG environment providing users with easy to access on-chip power supply monitoring, temperature monitoring, and precision analogue inputs.

“Many of our customers use the JTAG chain at the prototyping stage to very rapidly debug highly complex, densely populated printed circuit boards containing multiple BGA/FPGA devices,” added Dominic Plunkett. “Now, with these new Xilinx features, they can simultaneously monitor the FPGA power supplies and other analogue inputs to assess if they are performing within the required tolerances. Also, the thermal performance of the FPGA can be measured.”
The XJTAG development system is a cost-effective ‘out-of-the-box’ solution for debugging, testing and servicing electronic printed circuits boards and systems throughout the product lifecycle. The XJTAG system reduces the time and cost of board development and prototyping by allowing early test development, early design validation of CAD netlists, fast generation of highly functional tests and test re-use across circuits using the same devices.

XJTAG enables engineers to test a high proportion of the circuit (both boundary scan and cluster devices) including ball grid array (BGA) and chip scale packages, such as SDRAMs, Ethernet controllers, video interfaces, Flash memories, field programmable gate arrays (FPGAs) and microprocessors. XJTAG also enables In-System Programming of FPGAs, complex programmable logic devices (CPLDs) and Flash memories.

For more information about the XJTAG system, please telephone +44 (0) 1954 213888, facsimile +44 (0) 1954 211565 or email enquiries@xjtag.com. Alternatively visit www.xjtag.com.

Pricing for the XJTAG system ranges from £3,500 (£5,075) to £9,900 (£14,355).

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About XJTAG (www.xjtag.com)

XJTAG is a leading supplier of IEEE Std. 1149.1 compliant boundary scan development tools. Its JTAG (Joint Test Action Group) development system offers a highly competitive solution for designers and developers of electronic printed circuit boards and systems. Utilising XJTAG allows the circuit development and prototyping process to be shortened significantly by facilitating early test development, early design validation, fast development of functional tests and test re-use across circuits that use the same devices. XJTAG is based in Cambridge, UK, and is part of the Cambridge Technology Group.

What is JTAG?

Advances in silicon design, such as increasing device density and, more recently, ball grid array (BGA) and chip scale packaging, have made traditional electronic circuit testing methods hard to use. In order to overcome these problems and others; some of the world’s leading silicon manufacturers combined to form the Joint Test Action Group (JTAG). The findings of this group were used as the basis for
the Institute of Electrical and Electronic Engineers (IEEE) standard 1149.1: Standard Test Access Port and Boundary Scan Architecture.

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