Micron Level Placement Accuracy Case Studies for Optoelectronic Products

Daniel D. Evans, Jr., Zeger Bok
Palomar Technologies, Inc.
2728 Loker Avenue West
Carlsbad, CA 92010
Phone: (800) 854-3467 E-mail: info@bonders.com

Abstract
Applications requiring ultra high placement accuracies of 1µm to 3µm are resurfacing in several optoelectronic applications such as Arrayed Laser Print Head assemblies, P-Side Down Laser Attachment applications, and Multi-Channel Optical Communication products. An overview of the technologies, placement accuracies, and attachment methods is presented for two cases. With placement accuracies for surface mount machines typically around 40µm, 10µm for die attach machines, and 1µm for ultra high accuracy placement machines, this paper will cover the differences in measurement, material, and process controls that are required to successfully achieve ultra high placement accuracies of 3µm.

High Accuracy Die Attach Requirements and Challenges
The application breakout given in Table 1 is useful to explore general application, attachment, and accuracy requirements for ultra high accuracy die attach. The main breakout is by application product or technology. For the purposes of this paper, each of the applications explored is for specific attachment technologies (epoxy or eutectic) and general ranges of required placement accuracy.

Table 1 - High Accuracy Application Overview

<table>
<thead>
<tr>
<th>CASE</th>
<th>Attach</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCSEL Array</td>
<td>Epoxy</td>
<td>±3-5µm</td>
</tr>
<tr>
<td>P-Side Down Laser</td>
<td>Eutectic</td>
<td>±3-5µm</td>
</tr>
<tr>
<td>LED Laser Print Head</td>
<td>Epoxy</td>
<td>±2-5µm</td>
</tr>
<tr>
<td>Lithography/Screen Interconnect</td>
<td>Epoxy</td>
<td>±3-5µm</td>
</tr>
<tr>
<td>Thru Via Die Stacking</td>
<td>Misc.</td>
<td>±3-5µm</td>
</tr>
<tr>
<td>3D MEMS Stacking</td>
<td>Epoxy</td>
<td>±5-10µm</td>
</tr>
</tbody>
</table>

Terms and Definitions
Pick and place is composed of geometric accuracy and interconnect method. To completely define placement accuracy would require specifying all six (6) degrees of freedom, as shown in Figure 1. Most pick and place accuracy applications specify Z as a bond line and placement accuracy as X error, Y error, and Theta-Z error. For the purposes of this paper, the specific requirements will be listed for each of the cases studied.

Measurement Considerations
Measuring the actual placement accuracy down to 1-3µm requires both well characterized equipment and measurement methods [1]. Even if the equipment can support the resolution, the parts usually have imperfections beyond the

Figure 1 - Geometric Six Degrees of Freedom

Interconnects are comprised primarily of two methods for optoelectronic assemblies: adhesive (epoxy) or metallurgical (eutectic solder).

These attachment options can be either in-situ (serial) or batch (parallel). In-situ attachment is completed during the placement operation for each component and will have lower throughput since the attachment time for each component is added to the pick and place time. Batch attachment is completed after all components are placed so the actual attachment can be completed as a parallel process. Batch attachment methods typically have higher throughput compared to in-situ.

Another consideration for the attachment method is its effect on placement accuracy. To understand the effect on batch attachment methods, it is important to measure the pre-cure and post-cure accuracy of the components. In-situ attachment methods can have higher placement accuracy, especially if the design does not include self-centering.

Material and Process Considerations
When approaching micron level placement accuracies, there are several important factors that need careful management and control:

- Substrate flatness, cleanliness, and fiducial clarity (in particular in case of edge alignment)
- Die flatness, cleanliness, and fiducial clarity
- Attach material uniformity, shrinkage, symmetric application, and curing stability
targeted accuracy. Measurement methods must include ways to handle these imperfections.

The remainder of this paper will explore two cases for high accuracy placement and attach.

**Case 1: Multi-channel Communication Products (VCSELs)**

Several new products related to optical communications such as Active Optical Cables use multiple channels of transmit and receive pairs to produce the high bandwidth communication required for high performance computer connections or digital audio/video connections. The basic concept of an active optical cable link as shown in figure 2 is an optical cable that contains electrical input and output. The input conversion from electrical to optical (E-O) and the output conversion from optical back to electrical (O-E) is included as an integral part of the cable so that the end user sees only an electrical cable without the problems associated to optical cable connections [2]. The various optical to optical (O-O) interfaces as well as the actual fiber are also included in the cable. A complete cable as shown in figure 3 would include multiple channels for transmit and multiple channels for receive.

![Figure 2 – Active Optical Cable Schematic of one Transmission Path (Cables have Multiple Tx/Rx Pairs)](image)

One construction of a complete cable has an array of VCSEL transmitters which require high accuracy placement to allow better fiber optical coupling to the VCSEL lasers. These assemblies generally require photodiodes in the same package as well but these are easier to optically couple and require less placement accuracy.

The remainder of this case study will share geometry, accuracy, and attachment requirements of the VCSEL arrays.

The VCSELs used in this study are 300µm square by 200µm thick and are presented in 2x2 Gelpacks. The substrate can be any material but more even materials will produce more consistent results. The material in this study was a flexible circuit mounted to a PWB backing and presented in a common carrier in groups of 10 per carrier. The VCSELs are placed into 84-1LMIT1 epoxy which is deposited just prior to the pick and place process.

The arrangement of the VCSELs is shown in figure 4. VCSELs 5 through 1 are placed left to right according to a specified pitch. VCSEL number 5 is the master VCSEL and all others are placed relative to it. The required accuracy for each VCSEL is ±5µm in X and ±3µm in Y from the target location.

![Figure 4 – VCSEL Array, Gap X ±5µm, Gap Y ±3µm](image)

Placement results are evaluated pre-cured (wet) and post-cured to verify that shifting of the epoxy during cure does not adversely affect the results.

Pre-cure results are shown in figures 5 and 6. Statistical summaries of pre-cure results are given in Table 2. Pre-cure results are within specification for both X and Y.

![Figure 5 – Pre-cured (Wet) X Error Results](image)

![Figure 6 – Pre-cured (Wet) Y Error Results](image)
Post-cured results are shown in figures 7 and 8. Statistical summaries of post-cure results are given in Table 3. Post-cure results are also within specification for both X and Y.

Case 2: Wafer Scale – Eutectic Die to Wafer P-Side Down Laser Attachment

P-Side down laser attachment using eutectic solder is a mature process and has been used extensively for long haul and metro distance laser transmit modules [3]. The P-Side laser attach to heat spreader has traditionally been done using singulated heat spreaders with a pulsed heat in-situ reflow stage. The heat profile recipe is critical for proper solder phase in the final bond.

Recent work in P-Side down laser attachment has expanded the technology to Wafer Scale – P-Side Down Laser Die to Wafer attachment. This technology shifts away from singulated submounts to bonding directly on a wafer or on substrates. Design considerations for component heat flow, power, and reliability are significantly affected by the specific geometry, materials, and interconnect process. This case study will focus on pick and place and attachment capability. Substrate time at temperature and its effect on solder reflow and solder aging are explored as well. Measurement methods for P-Side down laser attachment provide some challenges during process development and will be covered as well.

The placement requirements are based on positioning the laser for optimal coupling of the laser optical output to coupling optics as shown in figure 9. The gray section represents the wafer substrate area upon which the laser will be solder attached. The wafer substrate has fiducials which determine alignment targets and gold pads plated with 80/20 AuSn eutectic solder. The laser is 300µm long by 250µm wide by 125µm thick with backside (P-Side) plated gold pads for solder attach. The P-Side of the laser provides alignment features that are a combination of fiducials and the alignment point edge. Both are referenced during the alignment phase using an upward looking camera.

The alignment specifications are defined in figure 9 and revolve around the P-Side intersection of the laser stripe location in the X direction and the laser output edge to substrate datum in the Y direction. Both X and Y directions have a ±3µm alignment tolerance. The angular alignment of the laser edge is also defined as a ±0.1degree tolerance in Theta-Z.
The pulsed heat tool is controlled through a temperature ramp profile as shown in figure 11. This is not the profile used for the study. While holding the laser in place on the wafer, the tool ramps from a background temperature to the reflow temperature, holds that temperature during the reflow time, and is then cooled down to the background temperature.

The pulsed heat tool used to pick the laser die includes the following capabilities and benefits:

- Pulsed heat controller
- Temperature up to 600°C
- Temperature accuracy ± 20°C
- Fast ramp (up to 65°C/s) - no overshoot
- Parts at high temperature for a limited time
- Programmable ‘point and click’ profiling

The wafer assembly process steps include:

- Load wafer onto steady state heated stage
- Load laser die (pre-flipped with P-Side down) onto machine
- Repeat the following process for all bond sites:
  - Vision find wafer at next available site
  - Vision find N-Side of next available laser die and pick it
  - Vision find P-Side of laser die on pick tool using lookup camera
  - Align and place laser die to substrate site
  - Apply bond force and initiate pulsed heat profile
  - Release laser die upon completion of pulsed heat profile including forced cooling cycle to below reflow temperature

Since it is not possible to directly measure the P-Side interface of the completed assembly, glass substrates were used for initial process development by measuring placement accuracy through the backside of the glass. The P-Side measurement results in figure 12 show that all samples were below ±3µm in the X and Y directions.

P-Side measurements are time consuming due to preparation of the sample materials and are nearly impossible to perform on actual wafer level substrates. To mitigate this problem, a correlation between P-Side and N-Side measurements was established which resulted in a more effective N-Side measurement specification of ±4.5µm in X and ±3µm in Y. The correlation was based on known misalignment errors between the lithography masks of both P-Side and N-Side of the wafer. All measurements could then be performed on a Nikon VMR3200 Automated Optical Inspection Microscope.

The wafer level substrate was then built and measured using N-Side measurement techniques as shown in the chart of figure 13. Most samples were within specification for both X and Y dimensions. Device level testing is normally required to determine actual yield.

Solder aging at temperature is typically not considered for singulated substrates since the solder is exposed to temperature for a short duration of time only. When moving to wafer level substrates however, solder can be exposed to background temperatures over 200°C for tens of hours depending on the number of bond sites and the equipment throughput.

Tables 4 and 5 provide a summary of the results from a study on the effects of exposure to time at temperature. A combination of time intervals at a background temperature of 230°C was used to evaluate both non-reflowed solder and reflowed solder in completed assemblies. The study involved...
waiting the pre-bond time intervals and then attaching a set of 4 laser die each. These laser die sets where then sheared after waiting the post-bond time intervals. This particular test sequence allowed testing of solder exposure to temperature before laser die attach (0 to 72 hours), solder exposure to temperature after laser die attach, and a combination of both (0 to 96 hours = Pre-bond Attach Time + Post-bond Shear Time).

Table 4 – Solder Attach Average Shear Strength vs. Time

<table>
<thead>
<tr>
<th>Shear Average [grams]</th>
<th>Post-bond Shear Time [Hrs]</th>
<th>Shear Time [Hrs]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>24</td>
</tr>
<tr>
<td>Pre-bond Attach Time [Hrs]</td>
<td>0</td>
<td>270</td>
</tr>
<tr>
<td></td>
<td>24</td>
<td>217</td>
</tr>
<tr>
<td></td>
<td>48</td>
<td>239</td>
</tr>
<tr>
<td></td>
<td>72</td>
<td>192</td>
</tr>
<tr>
<td>Grid</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

Table 5 – Solder Attach Range Shear Strength vs. Time

<table>
<thead>
<tr>
<th>Shear Range [grams]</th>
<th>Post-bond Shear Time [Hrs]</th>
<th>Shear Time [Hrs]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>24</td>
</tr>
<tr>
<td>Pre-bond Attach Time [Hrs]</td>
<td>0</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>24</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td>48</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>72</td>
<td>24</td>
</tr>
<tr>
<td>Grid</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

Table 4 shows a reduction in average shear strength from 270 grams to a minimum of 189 grams over all aging conditions compared to zero pre-bond attach time and zero post-bond shear time. Visual inspection of the sheared samples showed no observable differences in solder joint quality at 60X magnification.

Table 5 shows the effect on the range of shear strength for each data set. The data did not show continuing degradation of shear strength range for pre-bond attach time or post-bond shear time exposure.

Summary and Conclusions
Two separate optoelectronic application case studies have been reviewed. Both cases required ±5µm placement accuracy or better using adhesive or metallurgical attachment as shown in Table 6.

Table 6 - High Accuracy Application Cases

<table>
<thead>
<tr>
<th>CASE</th>
<th>Attach</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCSEL Array</td>
<td>Epoxy</td>
<td>±3-5µm</td>
</tr>
<tr>
<td>P-Side Down Laser</td>
<td>Eutectic</td>
<td>±3-5µm</td>
</tr>
</tbody>
</table>

Case 1: Multi-channel Communication Products (VCSELs)
The VCSEL based application placed an array of 5 VCSELs into epoxy. Post-cure results better than ±5µm in X and ±3µm in Y were achieved.

Case 2: Wafer Scale – Eutectic Die to Wafer P-Side Down Laser Attachment
The P-Side-Down 80/20 AuSn eutectic laser attach onto wafer produced results of ±3µm in X and ±3µm in Y for P-Side measurements on glass substrate. N-Side measurements on the wafer included shifts between N-Side and P-Side but results still indicated ±3µm in X and ±3µm in Y when N-Side measurements were correlated back to the P-Side.

The effect on solder quality of time at temperature was studied and found to have some effect on average shear strength. Additional studies could be completed to verify repeated results. Follow-on studies could be conducted on the reliability of laser devices as well.

Acknowledgments
Palomar Team members who contributed to equipment and process development include Mike Artimez, Don Beck, Tom Boggs, Bill Hill, Dan Martinez, Ricardo Saldana, and Tim Hughes.

References

Copyright ECTC(IEEE), May 2009, San Diego California