DESIGN FOR TESTABILITY – THE IMPORTANCE OF SIMPLE SOLUTIONS

By Holger Göpel, Chief Executive Director GÖPEL electronic

Since the very early days of electronic components failures have continuously been appearing. In spite of enormous development and production improvements this situation has not changed. Even automated equipment faults continue to be created on circuit boards. There is not a single manufacturing technique that will guarantee the 100 percent fault free circuit board. Each new technology creates new challenges and test methodologies to ensure fault free boards.

The increasing density and complexity of the components is a critical factor for producing faults.

However, the situation still remains the same; faulty assemblies must not be delivered and the requirement for testing is obvious.

Today, there are several test technologies, having their individual unique requirements and efforts. It doesn’t matter if it is the In-Circuit-Test (ICT), the Flying Probe Test (FPT), the Functional Test (FT), the Automated Optical Inspection (AOI) or the Boundary Scan Test, each technology has got its pros and cons. But one factor is going to be more and more decisive: the costs. But which costs are caused by which technology depends on the purchase costs and, essentially, on the effort to implement the test process. In the case of the latter there are costs for:

• test preparation
• test execution
• failure search.

Decisions should not always be exclusively based on costs. Analyzing the specifications are important to selecting the test technology as each has its own unique implementation problems.
Advantages and disadvantages of various test techniques

The disadvantages of the test techniques mentioned above are listed in the following:

FT:
• very intensive costs in test program creation (effort several weeks to months)
• very high costs to troubleshoot if a fault occurs – troubleshoot must be executed by well-trained personnel
• The testing of all functions and, obtaining 100 percent coverage of all possible faults is practically impossible

ICT:
• high costs in developing and preparing test object specific test-fixture (adapter)
• extra costs if a layout change is required
• storage and maintenance of the adapters very expensive
• probe (nails) placement becomes more and more difficult because of the density of circuit board traces
• the access to high lead count BGAs via nails is nearly impossible; it makes no sense to contact the pads because the advantage of very large-scale integration (VLSI) – namely the space saving – would be lost.

AOI:
• fault detection under components not possible
• electric faults cannot be detected

Flying Prober:
• high test times because of the sequential contacting of the test points
• maintenance costs for worn contact pins and moved mechanical components

“Test friendly” design of digital circuits

To reduce the disadvantages of the mentioned test technologies in the production test, it may be required to take advantage of component features that already exist in the circuits. The basic requirement is the development of a test concept with all required hardware and software elements in the unit to be tested. This endeavour is characterised as “test-oriented layout” or more commonly named “Design for Testability (DFT)”. 
If objects to be tested are investigated, one notices that the use of digital circuits have increased in the last few years. One example can be found in the modern consumer electronics. The trend from analogue to digital technology is obvious, especially indicated in the case of radios and TV sets. This trend must be considered when choosing the right test strategy, whereby the problems in testing in digital circuits are playing a decisive role.

There are two emphasis problems with the examination of digital circuits: test pattern generation and test verification.

The **test pattern generation** is characterized as a process for the production of stimulus signals for a circuit, in order to prove their correct function. The **test verification** is to determine the answering behaviour of the circuit. Simultaneously, the automatic test pattern generation and test verification has been becoming more and more difficult due to the increasing complexity of the boards. This can be clarified best when considering a functional test as example. Therefore it is assumed that each digital circuit is detachable into sequential and combinatorial circuit parts.

According to Moore and McCluskey, the minimum number of test vectors for a 100% functional test is calculated – in other words: how many test vectors are necessary to test all possible functions of a circuit - as follows:

\[ Q = 2^{(x+y)} \]

\( x = \) number of inputs

\( y = \) number of storage elements (sequential circuit parts)

For an assumed circuit with 25 inputs (x) and 50 internal latches (y), a test rate of 100ns per test steps requires a test time of \(10^7\) years.

This testing problem can be avoided by designing circuits which are more efficiently testable – using the sequential circuit parts. That means, the circuit must be designed to being able to be tested with an acceptable fault coverage and in an acceptable time and, furthermore, to overcome the problem of test access. This “test friendly” layout is called Design for Testability.
Subdividing the DFT

The Design for Testability must be subdivided into different groups: the Ad-Hoc-Design and the Structured Design.

Ad-Hoc-Design
The Ad-Hoc-Design contains the partitioning, the importation of additional test points and the use of bus architectures. Partitioning means the breakdown of the entire circuitry into circuit parts which are easier to test. The sum of the effort to test these part PCBs is considerably less compared to the effort in testing the entire circuit. Bus architectures simplify the testability by a selective activating of the individual bus participants.

Structured Design
The Structured Design’s aim is to reduce the sequential complexity of a network in order to simplify the test pattern generation and test verification. This aim is achieved by creating possibilities to control and observe sequential machine’s states. Methods, that implement these two types of a circuitry, are called “passive test aids”.

One of these passive test aids, which became accepted as systematic help and meanwhile is a standard for the manufacturers of mainframe computers, is the Scan Path method. Using this method, circuits with sequential storage elements can be subdivided into observable and controllable combinatorial circuit parts. Therefore, the storage elements’ internal states are required to be controllable and observable. This can be achieved by interconnecting the internal storage elements to shift registers, in order to enable the serial insertion of test items and the serial read-out of test answers. The classic among these methods is the LSSD (Level Sensitive Scan Design), which was developed by IBM for mainframe computers in the 1960s. It is based on the extension of functional storage elements to shift register elements, the so called “shift register latches” (SRL).

In normal operations the SRL works as latch (A=B=0) with data input D, clock input C and data output L1. In the test mode it takes the function of a shift register cell (C=0). The shift data input I is connected with the shift data output L2 of the previous cell. The data are switched from L2 to the I of the next cell. The clock inputs A/Master Clock and B/Slave Clock are set alternating and cause the shift process.
The Scan Path Method shows by the example of the LSSD that complex sequential circuits decompose into manageable, purely combinatorial circuits. Since combinatorial circuits, in contrary to sequential circuits, are testable with substantially fewer test vectors, test expenditure and testing time are significantly less.

The disadvantage of the sequential logic is changed into the advantage of its employment as part of the test machinery.

**Application to PCBs**

It seems logical that the described DFT facts, which have their roots in the circuit technology, also apply to PCBs to overcome test problems with these techniques. If the technology is applicable for circuits it must be transformed to assemblies. What is needed? Between the circuits test cells are required, which are switchable as shift chains as well as controllable and readable via few lines. If these test points are placed in the lines they are used for the In-Circuit Test. But the increasing complexity of todays boards demands the integration of these test points in the components to clear additional space for nets. This “test friendly” requirement is ideally met by Boundary Scan, also known as JTAG. Boundary Scan has been evolved to a standardised test of components and their interconnection networks.

**Boundary Scan - principle and employment**

Boundary Scan is possibly the most resourceful test technique which – in a similar way to the In-Circuit Test (ICT) but without physical contact – detects the failure location, sets thousands of test points – if necessary also under BGAs – and needs only four lines. While an ICT is only possible with specially constructed adapters, a Boundary Scan test is already useful if there is at least one Boundary Scan component on the board.

Boundary Scan essentially means “testing at the periphery (boundary)” of an IC. Besides the core logic and the contact points some additional logic is implemented in an IC. These test points are integrated between the core logic and the physical pins. The following image points it up graphically compared to the principle of the ICT.
Boundary Scan is simply and universally adaptable. In general one can argue that the technology supports the product throughout its entire life cycle. Already on the design stage, tests are possible by means of the CAD data, which also can be used later – even up to the customer’s application. That means that test pattern created for the design verification can be reused for the prototype debug and fabrication test. This is an important advantage since especially during the design of highly complex assemblies their testability for the future has to be considered.

Thus, the time and effort required for testing is enormously reduced. Only a few days or even hours are required to generate test programmes – compared with the high efforts which accompany an In-Circuit Test or Functional Test. Furthermore, the diagnosis times are minimized, not to mention the high production costs of nail bed adapters (some tens of thousands of EURO). Tremendous capacities and long storage times for these adapters can also be avoided.

Conclusion

Design for Testability – Boundary Scan is tailor-made for this key work. No other test technology is that dependent on the design. But what sounds like a problem is already a standard today, because all big manufacturers of components in principle include the Boundary Scan architecture in their ICs. The customers have already paid for this diagnostic aid, and would do a disservice to themselves if they would not use it. In particular in regard to the increasing complexity of the boards – and of course of the components themselves (BGA, μBGA, FlipChip) – Boundary Scan is the only solution for an extended testability and test coverage. “Designed to make a difference” is the advertising slogan of a big industry company. Boundary Scan meets this demand as no other test technology. You only have to use it.

The author:
Holger Göpel (57) had worked for Carl-Zeiss Jena in Jena/Germany in the department test engineering up to 1990. In 1990, together with some colleagues he founded the company GÖPEL electronic whose Chief Executive Director he has been since then. Meanwhile, GÖPEL electronic employs nearly 160 people, runs service and sales offices in Germany, France, UK and the US and maintains a worldwide distribution and service network with more than 300 additional specialists.