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FOR IMMEDIATE RELEASE

ASSET's European Design-for-Test Lab improves yields on prototype designs

Free testability analysis validates JTAG infrastructure in chips and printed circuit boards

Richardson, TX, and London, UK (February 12, 2007) - ASSET® InterTech, Inc., an international leader in boundary-scan (JTAG/IEEE 1149.1) test and in-system programming (ISP), has opened its first European Design-for-Test (DFT) Lab just outside of London. By validating the JTAG infrastructure in chip and printed circuit board designs, ASSET's DFT Lab reduces the time-to-market for new products by identifying JTAG testability issues before prototypes are assembled.

Building on the success of its recently-opened DFT Lab in the U.S., the European lab offers a free analysis along with design recommendations on pre-prototype designs. This analysis ensures that the JTAG infrastructure can be effectively deployed in its traditional structural test applications and in advanced applications that take advantage of the JTAG infrastructure, such as the testing of high-speed AC-coupled serial buses (IEEE 1149.6), Intel® Interconnect Built In Self Test (IBIST), system-level remote JTAG testing, concurrent programming based on the IEEE 1532 standard and others.

"In recent years as chip geometries have shrunk and board designs have gotten denser, boundary-scan test has become a critical tool for manufacturers. In fact, there are a number of advanced test and programming methodologies that take advantage of the JTAG infrastructure. These new test technologies can't perform their functions without a properly designed JTAG infrastructure," said Reg Waller, ASSET's European director. "By ensuring the soundness of a design's JTAG capabilities, the lab delivers systems to market faster. In the past, testability deficiencies were often not found until first samples or prototypes were built. Then, the deficiencies would have to be addressed and sometimes another round of prototypes built. This is a time-consuming process, but it can now be avoided."

ASSET's European DFT Lab is located at 6, Garden Court, Tewin Road, Welwyn Garden City, Herts AL7 1BH, UK. The free testability analysis is available to first-time users of boundary scan. Kent Zetterberg has been named manager of the lab. The analysis is performed with ASSET's DFT Analyzer™, the industry's only tool that automatically verifies the JTAG testability of board designs. The accuracy of a chip design's Boundary-

scan Description Language (BSDL) file is verified with the BSDL Validation Service, a collaborative effort of ASSET and Agilent Technologies, Inc. In addition, other tools can be applied to board and chip designs to validate their JTAG capabilities.

“We can offer a free first-time design analysis because DFT Analyzer, in most cases, reduces the weeks it takes to manually complete a testability analysis and produces a thorough report in a matter of hours,” Mr. Zetterberg said. “In addition, the reports we provide are not just simple test coverage reports which are typical of some test tools. Our analysis includes design recommendations that improve test coverage and ensure that the JTAG infrastructure embedded in a design can be utilized by other test and programming methodologies."

To contact ASSET's JTAG DFT Lab to arrange for a free JTAG design review, send an email to dftlab@asset-intertech.com or call +44 1707 396 056.

About ASSET InterTech

ASSET's boundary scan systems, ScanWorks® and DFT Analyzer, have advanced usability and automation features. ScanWorks has become the boundary-scan test system of choice for practically all major communication and defense/avionics suppliers, including Cisco, Ericsson, Motorola, Lucent, Alcatel, Tellabs, Huawei, Raytheon, Rockwell, Lockheed Martin, BAE, ITT, Northrop Grumman, Smiths and others. In addition, ScanWorks’ adoption by companies like Microsoft for its Xbox 360 video game console and Delphi for its automotive electronics demonstrates that ScanWorks will continue its leadership as boundary scan proliferates in computers, set-top boxes, consumer electronics, industrial controls, automotive and other industries.

ASSET InterTech, Inc. develops, markets, sells, and supports boundary-scan testability, in-system programming (ISP) and design-for-test products worldwide. ASSET's affordable ScanWorks and DFT Analyzer systems are easy yet powerful. ScanWorks allows users to quickly and easily test semiconductors, circuit boards or entire systems during every phase of a product's life, including design, manufacturing/repair and field maintenance and to program chips after they have been connected to a circuit board. DFT Analyzer is the industry’s first tool to validate the JTAG testability features of a design. ScanWorks and DFT Analyzer work in conjunction with a standard of the International Electronics and Electrical Engineering (IEEE) society known as the IEEE 1149.1 (JTAG) boundary-scan test specification. ASSET InterTech is located outside of Dallas, TX, at 2201 North Central Expressway, Suite 105, Richardson, TX 75080.

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