ABSTRACT
This paper investigates the reliability impact of copper-doped eutectic tin-lead (Sn-37Pb) alloys, in association with solder voiding, upon flip chip bumps. Previous work demonstrated that the addition of 1% copper in eutectic SnPb bump has significantly improve flip chip reliability against diffusion related failure mechanisms [1]. It is believed that additional copper doping should further improve flip chip reliability. Reflow experiments and differential scanning calorimetry analyses were conducted to determine feasible copper concentrations. Alloys with Sn-36Pb-XCu, where X is less than 4% were then evaluated through wafer bumping, flip chip assembly, and board-level reliability tests. Excellent results were obtained through each stage of the development. The reliability assessment tests included thermal cycle testing, high temperature storage (HTS), and high temperature operating life (HTOL) with test currents up to 600 milliams. Failure modes of interest include solder bump fatigue, under-bump metallization consumption, and electro-migration. Relatively large test die, 10mm x 10mm, with 250 and 200 micron pitches were used in the study. Flip chips were assembled to nickel-gold (NiAu) finish laminate boards having a thickness of 0.8mm. Substrate cleaning and standard underfill protocol assembly was followed.

A significant incidence of solder voiding was observed in the SnPbCu bumps and its effect upon reliability performance is also documented. X-ray analysis was used to statistically measure the incidence of solder voiding. The impact of solder voiding upon flip chip solder joint reliability has been a controversial topic. There is a concern that large solder bump voids; > 50% of the bump diameter, either created by poor pad wetting or poor bump processing, can lead to current crowding and poor solder bump features susceptible to early solder fatigue. Flip chips were prepared with an increased incidence of solder voiding during the bumping process and their reliability performance was compared to typical voided solder bumps from current production environment. The susceptibility of assembled flip chips to damage during handling was also evaluated by board-bending tests with typical-level and high incidence solder bump voiding. It is shown that the increased solder voiding does not significantly impact the reliability of the solder joints nor make them susceptible to damage from handling. However, the addition of Cu in the Sn-37Pb solder has significantly increased flip chip reliability, particularly against diffusion related failure mechanisms, regardless of the increasing level of bump voiding.

Key words: SnPbCu, flipchip, reliability, solder voiding

INTRODUCTION
Solder bump fatigue caused by the thermal CTE mismatch between the substrate and attached flip chips has been the main reliability concern for automotive flip chip packaging. Underfill technology [2] and continuous improvements in the material set: solder mask, solder flux, cleaning chemistry, conductor finish, as well as the associated manufacturing processes have made flip chips a superior packaging technology. Flip chip assemblies on laminate can provide low electrical inductance interconnects, low thermal resistance pathways, and significant cost advantages for high I/O count silicon die.

These improvements in solder bump fatigue resistance permit flip chips to survive hostile thermal environments, but have surfaced additional failure modes: electrical shorting from micro-voiding of underfill between solder bumps and solder bump diffusion-related mechanisms [3].

Irregular substrate features at solder bump attachment sites can cause underfill voiding in the region between solder bumps. These voids allow extrusion of the solder and with sufficient stress during thermal cycle testing, the extruding solder eventually generate electrical shorts. Solder bumps fully encapsulated with underfill will not extrude solder.

Solder bump diffusion-related failure mechanisms include: UBM (under bump metallurgy) consumption as well as both UBM and solder electro-migration. UBM consumption is the complete conversion of UBM metallization into IMC (inter-metallic compounds), such as Cu-Sn and Ni-Sn, resulting in high resistance bumps. The presence of a small amount of gold in the solder joint can accelerate the UBM consumption rate [4, 5]. Solder electro-migration is the migration of solder atoms in the direction of electron flow [6-8], while UBM electro-migration is the migration of the UBM metallization and IMC in the direction of electron flow [1, 9]. Both electro-migration mechanisms can generate high resistance bumps and localized current crowding can play an important accelerating role [10]. The crowding usually occurs at the corner of the aluminum conductor where it meets the solder bump. The peak current density at this interface can be several times greater than the average current density in the bump.
UBM consumption and UBM electromigration are more likely to occur when a thin film UBM, such as Al-Ni(V)-Cu, is used. Alternative UBM’s: electroplated copper mini-bump or electroless-nickel bump, provide better resistance to these diffusion related failure mechanisms, but have their own disadvantages. In general, a thin film UBM provides better bump thermal fatigue life, excellent protection to the underlying aluminum metallization, and is less likely to cause silicon crathing or passivation cracking.

The reliability of the metallurgy system, consisting of a eutectic SnPb bump over a Al-Ni(V)-Cu thin film UBM, is a function of the UBM thickness. A patented [11] approach for increasing the thickness of the UBM and thereby improving its reliability against diffusion is to use near eutectic SnPbCu solder with a copper concentration exceeding its ternary eutectic composition. The excess copper in the alloy precipitates along the UBM/solder interface as Cu-Sn IMC during the solidification (cooling) cycle of the bumping or assembly reflow process. The result is a thicker UBM containing an additional layer of Cu-Sn IMC over the original thin film UBM. It has been demonstrated that flip chip reliability increases significantly with the addition of 1% copper in the eutectic SnPb solder bumps [1]. It is believed that higher copper addition can further improve flip chip reliability.

The copper doping principle has been expanded to include copper concentrations up to 4% by weight in near eutectic formulations and is reported in this paper. There are two perceived limitations to increasing copper addition beyond the SnPbCu ternary eutectic composition. These are an increase of the liquidus temperature and increased incidence of solder bump voiding with increased copper content during bump formation and SMT assembly.

An increased liquidus temperature might require increasing the peak reflow temperature for eutectic solder, which is generally between 215°C and 230°C. Such a change is not permitted since it would require extensive and expensive soldering process verification for a large number of SMT components. The goal is to add a maximum amount of copper in the eutectic SnPb bump to maximize its resistance against diffusion related failure mechanisms without the need to modify the eutectic SnPb assembly reflow process.

Increased solder bump voiding was observed in the SnPbCu bumps with higher copper content by both mechanical cross-sections and X-ray analysis. Small and diffuse voids in solder bumps have not caused much concern in the industry. [12] Voiding at levels greater than 50% of the bump volume are known to adversely affect joint reliability and current flow performance. Voiding levels in flip chip bumps between these two levels has been a topic of discussion, concern, and study. [13, 14] The impact of increased solder bump voiding levels upon reliability performance is of special interest for the SnPbCu alloy.

The incidence of bump voiding can be directly affected by flux selection during wafer level processing. This technique was used to generate solder bumps with voiding levels exceeding those generated by typical production processing. Additionally, flip chip assemblies on laminate boards are most vulnerable to damage during board handling immediately following reflow assembly and prior to underfill dispense. A four-point board stress evaluation technique was used to evaluate the sensitivity of voided solder bumps to board-level handling stress. [15]

**TEST METHODOLOGY**

Three test chips were used in this study. The PST-2 is a power flip chip with 21 perimeter bumps on 0.46mm pitch. PB10 test die are daisy chained flip chips with 64 or 128 perimeter bumps on 0.25mm pitch. PB08 test die are daisy chained flip chip with 88 or 176 perimeter bumps on 0.20mm pitch. Two die sizes, 5mm x 5mm and 10mm x 10mm, for PB10 and PB08 were used.

Thermal cycling tests were used to determine the fatigue resistance of the bump alloys. Test die, PB08 and PB10, were either mounted on ceramic substrates with silver-based thick film conductor or 0.8mm thick laminate boards having NiAu trace finish. Two test conditions, -50°C/150°C (80 minutes per cycle) and -40°C/150°C (80 minutes per cycle), were used in the study. The temperature extreme dwell time was 15 minutes for each thermal cycle test.

A 150°C HTS test was used to study the impact of the bump alloys on UBM consumption. The test vehicle was a non-underfilled PST-2 on laminate board with NiAu finish. A die shear test followed by bump fracture surface analysis was used to determine the degree of UBM consumption damage at each end point.

HTOL tests were conducted to determine the impact of the bump alloys on solder electromigration and UBM electromigration. The test vehicle was an underfilled PST-2 on laminate with NiAu finish. Two test conditions, 350 mA and 600 mA bump currents, were conducted at 150°C.

One of the cost reduction methods in the semiconductor industry is die size shrinkage. However, the demand for bump current carrying capability and maximum operating temperature increases with die shrinkage. The ultimate goal is to achieve 1000 hours of HTOL test at 1,000mA/150°C to accommodate the perpetual die shrinkage trend.

The incidence of bump voiding is most easily measured by X-ray imaging, which generates an “integrated cross-sectional” view of the voiding within a given bump. The amount of voiding in each bump of a test die is cataloged into 10-30%, 30-50%, or greater than 50% of the bump diameter. A solder voiding percentage is then reported for each die as the number of solder bumps having a voiding level greater than 10% of the bump diameter.

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The four-point board stress evaluation technique was used to determine the sensitivity of assembled flip chips to board-level stress. The test vehicle was a non-underfilled PB10 on a prepared laminate 25mm x 100mm test coupon having the die orientated 45° to the board axis. This orientation generates maximum stress at the corner vertices. The coupon was instrumented with a biaxial strain-gage and the die daisy-chain with continuity contacts to measure the point of solder damage. The four-point fixture generates uniform stress over the coupon surface as the coupon is bent at a constant slow rate that allows the tensile force to strain the corner bumps. An increase in the daisy-chain resistance occurs at the point of crack initiation. The point of damage is recorded at a resistance increase of 10%.

RESULTS AND DISCUSSION
From preliminary wafer bumping and flip chip assembly experiments, near eutectic SnPbCu alloys containing up to 4% copper were found to be compatible with the eutectic SnPb reflow processes. The liquidus temperature of these Cu doped alloys can be higher than the peak reflow temperatures (205°C to 225°C) used during assembly, see Table 1. This is a contradiction to the conventional soldering practice, which assumes that the peak reflow temperature must be 20°C to 50°C above the liquidus temperature of the solder alloy.

DSC analyses (Figures 1 through 3) and the metallurgical analyses from a previous study [1] indicate that near eutectic SnPbCu alloys with up to 4% copper are essentially in a liquid state consisting of liquid near eutectic SnPbCu and a very small amount of CuSn IMC particles suspended in the liquid solder. Apparently the presence of small amounts of IMC particles has no adverse impact on the reflow characteristics of the SnPbCu alloys. For practical purposes, during bumping or circuit board assembly reflow, near eutectic SnPbCu alloys with up to 4% Cu can be treated as eutectic SnPb.

Table 1. Solidus and Liquidus Temps. of SnPbCu Alloys

<table>
<thead>
<tr>
<th>Alloy</th>
<th>Solidus (°C)</th>
<th>Liquidus (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>63Sn-37Pb</td>
<td>182.7</td>
<td>182.7</td>
</tr>
<tr>
<td>62Sn-36Pb-2Cu</td>
<td>183.0</td>
<td>183.0</td>
</tr>
<tr>
<td>61Sn-35Pb-4Cu</td>
<td>180.6</td>
<td>337.1</td>
</tr>
</tbody>
</table>

Wafer Bumping
As shown in Figure 4, bump alloys with up to 4% Cu were successfully deposited on the test wafer using the solder paste bumping technology. However, the level of bump voiding was found to increase with copper concentration, see Table 2, in particular when the Cu content exceeded 3%.
There are many other factors, such as flux, reflow profile, etc., that can also affect bump voiding. After several DOEs, Sn-36Pb-2.5Cu was selected for further evaluation for circuit board assembly and flip chip reliability. The target Cu composition is 2.0% to 3.0%. After optimizing the solder paste formulation and wafer bumping reflow process, the voiding level of Sn-36Pb-2.5Cu vs. Sn-37Pb bumps at the wafer level were collected in the production environments. Wafers were analyzed with a real time X-ray, and any voids larger than 10% of the bump diameter were recorded as a bump with solder void. The level of bump voiding is 0.8% and 10.6% for Sn-37Pb and Sn-36Pb-2.5Cu, respectively. In this study, the co-relation between bump voiding and reliability was closely followed and analyzed in the subsequent reliability tests and experiments.

<table>
<thead>
<tr>
<th>Cu Content</th>
<th>0% Cu</th>
<th>2% Cu</th>
<th>3% Cu</th>
<th>4% Cu</th>
<th>6% Cu</th>
</tr>
</thead>
<tbody>
<tr>
<td>% Voiding</td>
<td>0.0</td>
<td>0.1</td>
<td>0.4</td>
<td>23.9</td>
<td>21.5</td>
</tr>
</tbody>
</table>

Figure 4. SnPbCu bumps with various Cu compositions were successfully deposited on test wafers using a solder paste wafer bumping process.

Table 2. Bump Voiding vs. Copper Concentration
Flip Chips Assembled to Ceramic Substrate

ASSEMBLY & METALLURGICAL ANALYSIS
The selected solder alloys were bumped on test wafers using a solder paste bumping technology [16]. One advantage of this bumping technology is the ability to accurately control the solder bump composition. Test die were then assembled on various test boards for reliability evaluations. Typical eutectic SnPb reflow processes with peak reflow temperatures between 205°C to 225°C were used for SMT assembly. The test substrates were then cleaned and underfilled as necessary. A total of 3500 die were assembled on various substrates.

There is little difference in assembly yield between Sn-37Pb and Sn-36Pb-2.5Cu flip chips. The assembly yields were 99.4% and 99.6% for the Sn-37Pb and Sn-36Pb-2.5Cu flip chips, respectively. The causes of rejects are mostly handling related issues in a laboratory environment, such as misalignment and mechanical damage, and not related to alloy composition.

The cross-section of a Sn-36Pb-2.5Cu bump assembled to a laminate substrate with NiAu finish is shown in Figure 5. The Sn-36Pb-2.5Cu bump has excellent solderability and good bump formation around the substrate conductor. A close-up view at the solder/UBM interface shows that there is a continuous layer of CuSn IMC. The average thickness of the IMC layer is around 3 to 5 microns vs. 1 to 2 microns for the Sn-37Pb bump. The thicker IMC layer at this interface has significantly increased flip chip reliability as shown in the following reliability tests.

Figure 5. Cross-section of Sn-36Pb-2.5Cu bump assembled to a laminate substrate. The close-up of the UBM shows the CuSn IMC layer at the interface is 3 to 5 microns thick.

Thermal Cycle Test I
The purpose of these tests was to determine the relative thermal fatigue life of near eutectic SnPbCu bumps containing 1%, 2%, and 3% copper. The relative thermal fatigue life of non-underfilled Sn-37Pb bump on bare ceramic substrate was set arbitrarily to 1.0. Non-underfilled PB10 test die (5mm x 5mm) on rigid ceramic substrate was chosen as the test vehicle, because the thermal fatigue resistance of a bump alloy is easier to measure without any complicating factors introduced by underfill quality or variability.

The results of -50°C/150°C thermal cycle test are given in Table 3 and Figure 6. Based on Weibull analysis using a 95% confidence bound, there is no statistical difference between the thermal fatigue lives of all four alloys. In other words, addition of up to 3% copper to the Sn-37Pb bump does not have any measurable impact on flip chip thermal fatigue reliability.

As shown in Figure 12, the failure mechanism is solder fatigue near the bump/UBM interface due to global thermal mismatch between the test chip and the ceramic substrate, and local thermal mismatch between the test chip and the bump solder. This is the typical failure mechanism for this type of test vehicle.
Table 3. Thermal Cycle Test Results

<table>
<thead>
<tr>
<th>Alloy</th>
<th>Weibull Life (cycles)</th>
<th>Relative Reliability</th>
</tr>
</thead>
<tbody>
<tr>
<td>63Sn-37Pb</td>
<td>1503</td>
<td>1.00</td>
</tr>
<tr>
<td>Sn-37Pb-1Cu</td>
<td>1721</td>
<td>1.15</td>
</tr>
<tr>
<td>Sn-36Pb-2Cu</td>
<td>1491</td>
<td>0.99</td>
</tr>
<tr>
<td>Sn-36Pb-3Cu</td>
<td>1652</td>
<td>1.10</td>
</tr>
</tbody>
</table>

Thermal Cycle Test II
The purpose of the test is to demonstrate that Sn-36Pb-2.5Cu bump is reliable for under-hood automotive applications. It is required to pass 1000 cycles of -40°C/150°C thermal cycle test. Eutectic SnPb bump was not able to pass the test due to UBM consumption when attached to circuit boards with NiAu finish.

As shown in Figure 9, the failure for PB08 test die with Sn-36Pb-2.5Cu bump is cause by underfill cracking. The cracks initiated at the corner of the flip chip and then extended to the flip chip/underfill interface resulting in solder fracture in the bumps. The underfill process used for this experiment was found to be marginal for the 0.2mm pitch devices.

As documented in Table 4, Sn-36Pb-2.5Cu bumps have a higher incidence of voiding than Sn-37bumps at the wafer level. However after assembled to the circuit boards, the difference in bump voiding in not noticeable between these two bump alloys. Most of the solder voiding observed is under 30% of the bump diameter and none of the bump voiding is larger than 50% of the bump diameter. Among the four groups of test boards, PB10 with Sn-36Pb-2.5Cu has the highest level of bump voiding. However, this is the group that demonstrated the best reliability in the test.

Table 4. Thermal Cycle Test II Results

<table>
<thead>
<tr>
<th>Device</th>
<th>Alloy</th>
<th>Voiding (Die)</th>
<th>Voiding (Board)</th>
<th>500 cycles</th>
<th>1000 cycles</th>
<th>1500 cycles</th>
<th>3000 cycles</th>
<th>Failure Mech.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB10</td>
<td>SnPbCu</td>
<td>12.1%</td>
<td>10.3%</td>
<td>0/119</td>
<td>0/119</td>
<td>0/115</td>
<td>0/115</td>
<td>UBC</td>
</tr>
<tr>
<td>PB10</td>
<td>Sn-37Pb</td>
<td>~1%</td>
<td>9.5%</td>
<td>0/48</td>
<td>28/48</td>
<td>0/120</td>
<td>0/120</td>
<td>UBC</td>
</tr>
<tr>
<td>PB08</td>
<td>SnPbCu</td>
<td>9.6%</td>
<td>3.5%</td>
<td>0/120</td>
<td>29/116</td>
<td>29/116</td>
<td>29/116</td>
<td>UF Crack</td>
</tr>
<tr>
<td>PB08</td>
<td>Sn-37Pb</td>
<td>~1%</td>
<td>4.4%</td>
<td>0/48</td>
<td>37/48</td>
<td>37/48</td>
<td>37/48</td>
<td>UBC</td>
</tr>
</tbody>
</table>

Failure analysis results are shown in Figures 8 - 9. The failure mechanism for Sn-37Pb bump is UBM consumption (UBC). As can be seen in Figure 8B there is no sign of solder fatigue cracking or any other damage in the cross-section of the failed Sn-37Pb bump. However, fracture surface analysis, see Figures 8C and 8D, reveals that the failed Sn-37Pb bumps has separated from the flip chip at the Ni(V)-Al interface due to the complete consumption of Cu-Ni(V) thin film UBM by Sn in the solder. This is a typical failure mechanism for Sn-37Pb bumps attached to circuit boards with NiAu finish. One of the solutions is to add Cu in the Sn-37Pb bump to increase its resistance against this diffusion related failure mechanism.
fracture at the Ni(V)-Al interface or the results of UBM consumption.

**Figure 9.** Fracture underfill has caused SnPbCu PB08 failure. The underfill process needs to be optimized.

**Thermal Cycle Test III**

Another experiment was designed to evaluate the impact of bump solder voiding where the level of voiding of Sn-36Pb-2.5Cu was artificially increased by employing an alternate flux known to generate excessive voiding during bump formation at the wafer level. Two special lots of flip chips were prepared, Lot 1 had lower voided solder bumps, whereas Lot 2 had excessive voiding. Several die of Lot 2 had >50% voiding before assembly. Interestingly the solder voiding level decreased during the reflow assembly process. Representative X-rays of assembled Lot 1 and Lot 2 die are shown in Figure 10 and 11 respectively.

The test assemblies were underfilled PB10 (10mm x 10mm) on laminate, subjected to –40°C/150°C testing and results are given in Table 5. The die were failure free up through 2500 cycles. The failure mode occurring before 3000 cycles was underfill cracking with some accompanying underfill micro-voiding, see Figure 12. These results show that when the flip chip bump voiding is less than 50% of the bump diameter, the otherwise high voiding level does not impact thermal cycle testing reliability. The observed failure modes were not related to solder bump voiding.

**Table 5.** Thermal Cycle Test III Results

<table>
<thead>
<tr>
<th>Device</th>
<th>Voiding (Die)</th>
<th>Voiding (Board)</th>
<th>1000 cycles</th>
<th>2000 cycles</th>
<th>2500 cycles</th>
<th>3000 cycles</th>
<th>Failure Mech</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB10 – Lot 1</td>
<td>32%</td>
<td>21%</td>
<td>0/75</td>
<td>0/72</td>
<td>0/72</td>
<td>0/72</td>
<td></td>
</tr>
<tr>
<td>PB10 – Lot 2</td>
<td>38%</td>
<td>28%</td>
<td>0/75</td>
<td>0/72</td>
<td>0/72</td>
<td>0/72</td>
<td>UF Crack</td>
</tr>
</tbody>
</table>

**Figure 10.** X-ray of Lot 1 - Sn-36Pb-2.5Cu Bumps

**Figure 11.** X-ray of Lot 2 - Sn-36Pb-2.5Cu Bumps

**Figure 12.** Solder Extrusion into Underfill Micro-void

The incidence of underfill micro-voiding is due to the irregular surface features of the laminate board as the solder mask defines the solder pad geometry. The “trough” that is formed at the solderable pads can trap air, degas, and in general impede the flow of wicking underfill, see Figure 13. Although not utilized in these tests, conductor defined solderable pad geometries eliminate both the soldermask and the generation of underfill micro-voiding.

**Substrate Bend Testing**

A high incidence of solder voiding could negatively impact the board handling strength of assembled flip chips on laminate substrates. Both Lot 1 and Lot 2 Sn-36Pb-2.5Cu test die, six samples each, were assembled to test coupons designed for four-point board level testing as previously described. Assembled die that can withstand a 1000 micro-strain level are considered robust for typical assembly handling. The results for this testing are given in Figure 14 and clearly show that the excessive level of voiding of Lot 2 parts does have an impact on the assembly strength, but does not put the assemblies at risk.
HTS Test
The purpose of the test was to determine the impact of alloy composition on UBM consumption. Non-underfilled PST-2 on laminate board with NiAu finish was used as the test vehicle. The test condition is high temperature storage at a constant temperature of 150°C. In the test, parts were end pointed every 250 hours for the first 2000 hours of test, and every 500 hours thereafter. At each end point, test chips were sheared off their substrates and the bump fracture surfaces were examined with SEM to determine the fracture mode. The typical fracture mode is ductile shear fracture in the solder. However, brittle fracture will occur at the Al-Ni(V) interface, when the Ni in the Ni(V) layer has been completely converted into Ni-Sn IMC. The tin in the solder does not bond to the aluminum metallization on the flip chip resulting in delamination between the Ni-Sn IMC layer and the aluminum metallization. Under this condition, the aluminum in the UBM will become visible on the bump fracture surface at the chip side. The presence of the brittle fracture at the Al-Ni(V) interface indicates that the UBM has been consumed or damaged.

Onset of degradation is defined as the first end point when UBM consumption is detected. UBM consumption damage usually starts at the perimeter of the bump, and progresses toward the center of the bump after further exposure to elevated temperature. Eventually the entire UBM will be consumed resulting in a resistive or open bump.

The results of the HTS test are shown in Table 6 and Figure 15. As can be seen, severe UBM consumption has occurred in Sn-37Pb bumps after 500 hours of test, while no sign of damage could be found in the near eutectic SnPbCu bumps after 4000 hours of test. The resistance to UBM consumption also increases with the increasing Cu concentration in the SnPbCu bumps. The onset of degradation is estimated to be around 250 hours and 5000 hours for the Sn-37Pb bumps and the Sn-36Pb-2.0Cu bumps, respectively, see Table 6. The copper Cu addition to the eutectic SnPb bumps has effectively slowed down the UBM consumption failure mechanism. It is believed that the proeutectic Cu-Sn IMC layer deposited on top of the original UBM acts effectively as a diffusion barrier that slows the arrival of Sn to the Al-Ni(V) interface.

<table>
<thead>
<tr>
<th>Bump Alloy</th>
<th>Onset of Degradation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sn-37Pb</td>
<td>250 hours</td>
</tr>
<tr>
<td>Sn-36Pb-2.0Cu</td>
<td>5000 hours</td>
</tr>
<tr>
<td>Sn-36Pb-2.5Cu</td>
<td>&gt;6000 hours</td>
</tr>
<tr>
<td>Sn-36Pb-3.0Cu</td>
<td>&gt;6000 hours</td>
</tr>
</tbody>
</table>

Figure 15. Bump fracture surface analysis reveals UBM consumption damage after 150°C HTS test. Test die were sheared off circuit board, and the bump fracture surfaces were analysis with SEM.

HTOL
The purpose of the test was to determine the electromigration resistance of the SnPbCu bump alloys under 350mA/150°C and 600mA/150°C test conditions. Underfilled PST-2 test die assembled to laminate board with NiAu finish was used as the test vehicle. The Sn-37Pb bump is capable of carrying 250mA at 140°C maximum junction temperature. It does not qualified for 150°C application due to UBM consumption as discussed in the previous section.

The first HTOL test used a 350 mA bump current, 147°C ambient temperature, with 150°C-152°C bump temperature. The second used a 600 mA bump current, 145°C ambient temperature, with 150°C-155°C bump temperature. With a passivation opening of 127µm in diameter, the current densities were approximately 2760 and 4740 A/cm², respectively.

The results are shown in the Table 7 with Figures 16 and 17. In a 350mA/150°C HTOL test, the Sn-37Pb bumps failed to pass 1000 hours of test, and have almost 100% failure rate after 1500 hours of test, while no failure was observed in Sn-36Pb-2.5Cu bumps after 4000 hours of test. The bump solder voiding in the Sn-36Pb-2.5Cu test boards is three times of those in Sn-37Pb test boards. This indicates that solder bump voiding has little effect on flip chip reliability in HTOL test. The results of another 350mA/150°C HTOL test is shown in Figure 16, as can be seen the Weibull lives of Sn-37Pb and Sn-36Pb-2.5Cu are 1280 hours and 13,700 hours, respectively. This is a more than ten-fold improvement in reliability. Similar results are observed in a
ceramic and laminate substrates with very high yields. The presence of additional copper greatly improves the high temperature operating life by impeding the cap consumption diffusion process for bumps joined to a thin film Al-Ni(V)-Cu UBM. The copper greatly improves electrical conductivity by arresting the electromigration fault under high current conditions at 150°C, and it significantly improves the thermal cycle life of flip chips on laminate substrates when evaluated under –40°C/150°C conditions. The failure mechanisms are documented and well understood for these testing methods.

The concerns for the higher liquidus temperatures and the higher incidence of solder bump voiding for copper doped eutectic tin-lead alloys have been addressed and are shown to be of minor consequence. Excellent reliability results were obtained from near-eutectic bumps having a 2.5% copper content with well over 10% of bumps having voids. Solder bumps intentionally created with increased voiding still provided greater than 2500 cycles of performance under –40°C/150°C thermal cycle conditions.

It is shown that the increased solder voiding does not negatively impact the reliability of the solder joints nor make them susceptible to damage from handling. Therefore the addition of copper to Sn-37Pb solder has significantly increased flip chip reliability, particularly against diffusion related failure mechanisms, regardless of the increasing level of bump voiding.

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REFERENCES

CONCLUSIONS
This paper has documented the development and reliability impact of copper doped eutectic tin-lead alloys for flip chip applications on ceramic and laminate substrates. An optimized alloy composition of up to 3% copper can readily be used to form a flip chip bump during wafer bumping requiring no special thermal treatment during solder reflow formation or assembly processing. The formed copper-doped near-eutectic bump can be readily assembled to

Table 7. Results of 350mA/150°C HTOL Test

<table>
<thead>
<tr>
<th>Alloy</th>
<th>Voiding (Die)</th>
<th>Voiding (Board)</th>
<th>1000 hrs</th>
<th>1500 hrs</th>
<th>2000 hrs</th>
<th>4000 hrs</th>
<th>Failure Mech.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SnPbCu</td>
<td>10.7%</td>
<td>18.4%</td>
<td>0/72</td>
<td>0/72</td>
<td>0/72</td>
<td>0/72</td>
<td>UMC/EM</td>
</tr>
<tr>
<td>Sn-37Pb</td>
<td>0.8%</td>
<td>6.2%</td>
<td>4/24</td>
<td>22/24</td>
<td>22/24</td>
<td>22/24</td>
<td></td>
</tr>
</tbody>
</table>

Figure 16. Results of a 350mA/150°C HTOL test. The Weibull life of Sn-37Pb and Sn-36Pb-2.5Cu are 1,280 hours and 13,700, respectively.

Figure 17. Results of a 600mA/150°C HTOL test. The Weibull life of Sn-37Pb and Sn-36Pb-2.5Cu are 793 hours and 7,156, respectively.

600mA/150°C HTOL test. As shown in Figure 17, The Weibull lives for Sn-37Pb bumps and Sn-36Pb-2.5Cu bumps are 793 hours and 7,156 hours, respectively. This is a nine-fold improvement in reliability. In fact, this SnPbCu bump is capable of surviving 1000 hours of 600mA/150°C HTOL. The first failure in this test occurred at 3200 hours of test. Apparently, the copper addition in the eutectic SnPb bump has significantly improved flip chip reliability regardless of the increasing level of solder voiding.


