Test more, pay less

The integration of JTAG/Boundary Scan into Aeroflex’s 5800 Series Multi-functional ATE System enables high Test Coverage, short Test Times and saves Money

Introduction
The importance of quality management, quality products and quality assurance continuously increases. New technologies and products make higher demands to the manufacturing process. The most important goals of today’s electronics production are to control modern processes as well as assure a high quality level. The right test strategy is the linchpin to meet these demands.

The following article provides an example, starting in the PCB production process, analysing possible faults and showing how to optimise test and fault coverage.

Modern Test Opportunities
Today there is a multitude of test technologies. The following table shows the most common and best known listed in chronological order and due to their principle.

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Table 1 Modern Test Methods

The principle of an optical or electric test technology is critical for its possible utilisation to detect faults. An optical method is logically able to detect visible faults, e.g. missing components, wrong placement or wrongly polarised components. The opportunity of a qualitative evaluation of solder joints is particularly noteworthy. An optical test principle’s limits lie in the electric field. Of course, by only using this methodology, it’s impossible to make a statement about a component’s correct function.

On the contrary, the correct performance of a component can be verified by electrical test, for example if a resistor is correct or an IC’s output driver works. Free access to the assembly or the single component pins is not necessary for each electric test method, unlike MFT. This principle can’t make qualitative evaluation about a solder joint or isn’t able to detect a mechanical component defect.
Each test technology has its advantages and disadvantages. Nonetheless, if it’s about speed, test coverage or mechanical access – no single test method can be seen as a universal remedy. That’s why it makes sense to combine different test methodologies.

**Combination of Boundary Scan and MFT**

When specifying Aeroflex’s 5800 Series Multi-functional test system, the integration of JTAG/Boundary Scan was critical to guarantee high test coverage for only partly contactable assemblies. Because the development of digital functional test modules for complex components is time consuming and expensive, it’s more convenient to test ID codes as well as correct mounting and soldering of a component via Boundary Scan instead of testing the component function.

JTAG/Boundary Scan can be explained most simply using In-Circuit Test as an example. Both are purely electric test technologies with the same principle. The conductor paths (nets) are stimulated at one point and measured at another point. Information based on this measurement infers potential faults on a PCB. The main difference between Boundary Scan and ICT is their access to the nets. While the ICT needs to contact the tracks mechanically via predefined test points on a board, Boundary Scan is a purely electronic method that applies additional logic which is integrated into many complex components. A Boundary Scan IC’s architecture is displayed in the following image:

![Image 1: Typical Boundary Scan IC](image)

The necessary information transfer between test system and Boundary Scan component is executed via a four-wire test bus, which must be included in the PCB design. A test system therefore only needs a connection for this test bus.

Image 1 shows, that the Boundary Scan cells are located between component pins and its core logic. The inner component logic doesn’t play a role for testing circuits on an assembly any longer, regardless of whether it’s a processor or PLD. Layout display is simplified as test points are not or barely required (image 2).
The Integration Solution

In order to simplify the integration of other vendors’ test and measurement instrumentation into the 5800 Series Multi-functional test system, market standard open software and hardware platforms were selected.

The Aeroflex chassis utilises an MXI-4™ card for communication with the PC, a 3U PXI backplane to integrate any PXI modules, combined with a special Aeroflex backplane for internal signals at fast In-Circuit test as well as analogue and digital functional test.

The interactive open software environment AIDE (Aeroflex Integrated Development Environment) allows for the integration of .NET compliant “third party software”, e.g. Teststand™, Labview™, C#™, or VB.NET™.

- Each .NET programming environment has access and can control the hardware of the 5800 multi-functional test system
- AIDE can use the code, generated in a .NET programming environment during development or sample test, for PCB testing
- Systems with DLL, .NET or Active X drivers can be controlled with AIDE
- Programs, created with AIDE, can be executed in each .NET capable software environment
- Older not .NET compliant drivers can also be integrated by means of tools included in the software

Image 4: Aeroflex Integrated Development Environment

The digital functional test subsystem of the 5800 supports the JTAG/Boundary Scan standard (IEEE 1149.4) and can be combined with a Boundary Scan system from GOEPEL electronic. The integrated Boundary Scan hardware consists of a PXI or PCI controller, a TAP Interface Card (TIC) and various I/O modules. By utilising digital and analogue I/O modules the multi-functional test system’s test coverage is significantly increased. The controller’s architecture supports data rates up to 80 MHz and up to eight independent TAP (Test Access Ports).

The Boundary Scan test programs can be controlled by the AIDE development environment. This is beneficial, as programs, generated for new developments or prototype tests, can be reused in production tests.

During the Boundary Scan test, the vectors can be switched directly to the UUT via DTP cards and additionally stimulate the test object, can check the behaviour of peripheral components and set them high-impedance or configure if applicable. The transparent handling of the fault report by the AIDE environment therefore enables a complete integration into the test program.
The predefined test opportunities of GOEPEL electronic’s SYSTEM CASCON™ Boundary Scan software can be extended by integration into the 5800 digital test system. All 5800 Digital Test Point (DTP) cards feature Boundary Scan cells, and thus, can be utilised like a Boundary Scan component with input and output pins. Hence, non Boundary Scan circuits on the board, which are contacted by Aeroflex DTP test pins, can be used for a Boundary Scan test.

The DTP card’s test pins are organised in four groups with 16 test pins each. The configuration for each group is described in a BSDL file. These BSDL files are integral part of the 5800 system software. All other TDI and TDO are connected internally.

The DTP’s TAP features five pins on the card interface and can be used as follows:

1st The resulting Boundary Scan chain is configured as separate chain with it’s own TAP of the Boundary Scan controller or
2nd is connected in series with the UUT’s Boundary Scan chain.

If several DTP cards are utilised, they can be assembled in a series in the adapter in the Boundary Scan mode.

If the DTP card is configured in Boundary Scan mode, the four blocks with 16 test pins form a single Boundary Scan chain. Each block can be set separately. If a block is switched in BYPASS mode, the test pins act as normal digital pins, and are controlled by the Digital Test Controller (DTC) r and the DTP test pin instructions. The subdivision into four blocks therefore enables the utilisation of Boundary Scan controlled stimulus and response pins as well as normal digital test points on a digital test point card at the same time.

Programs and tests, developed by the SYSTEM CASCON™ tool suite, can be directly executed by means of the SYSTEM CASCON™ Boundary Scan library in the AIDE program. All methods and variables are defined in the library. Using the modules in the library, users can execute specific tests according to their requirements.

![Image 5: Boundary Scan and Digital Functional Test conjointly](image)
The circuit arrangement shows the joint utilisation of Boundary Scan and digital functional test. There are no test pads at the left component pins of the Non-Scan DUT. That means, pins can only be controlled via IC_1 and IC_2 (Boundary Scan). On the pins on the right, there are test pads but no Boundary Scan component (Functional Test). The non-scan component can only be tested by the joint utilisation of Boundary Scan and Functional Test.

**Summary**

Not only test and repair engineers benefit from a synthesis of Multi-functional Test and Boundary Scan but also the PCB design. Furthermore, throughput, test and production costs can be targeted to be reduced earlier and still give extensive fault detection. Another advantage of these test technologies’ combination is the constant improvement of the production process of prototypes and series production by possible isolation of fault sources, and therefore ideal support with quality management.